Dolby Pro-Logic Surround Matrix Decoder

SSM-2125/SSM-2126

FEATURES

Noise Generator and Autobalance Circuits are Contained On-Chip
Autobalance On/Off Control
4-Channel Pro-Logic and Dolby 3 (Surround Channel Defeat) Modes Available
Selectable Center Channel Modes—Normal, Wideband, Phantom, Off
Direct Path Bypass (Normal 2-Channel Stereo Mode)
Wide Channel Separation
Center to Left, Right Channels—35 dB min (SSM-2125)
Any Channel to Another—25 dB min (SSM-2126)
Wide Dynamic Range—103 dB typ
Low Total Harmonic Distortion—0.02% typ
Available in a 48-Pin Plastic DIP
CMOS and TTL Compatible Control Logic

APPLICATIONS

Direct View and Projection TV
Integrated A/V Amplifiers
Laserdisc and CD-V Players
Video Cassette Recorders
Stand-Alone Surround Decoders
Home Satellite Receiver/Descramblers

GENERAL DESCRIPTION

The SSM-2125 and SSM-2126 are Dolby* Pro-Logic Surround Decoders developed to provide multichannel outputs from Dolby Surround encoded stereo sources.

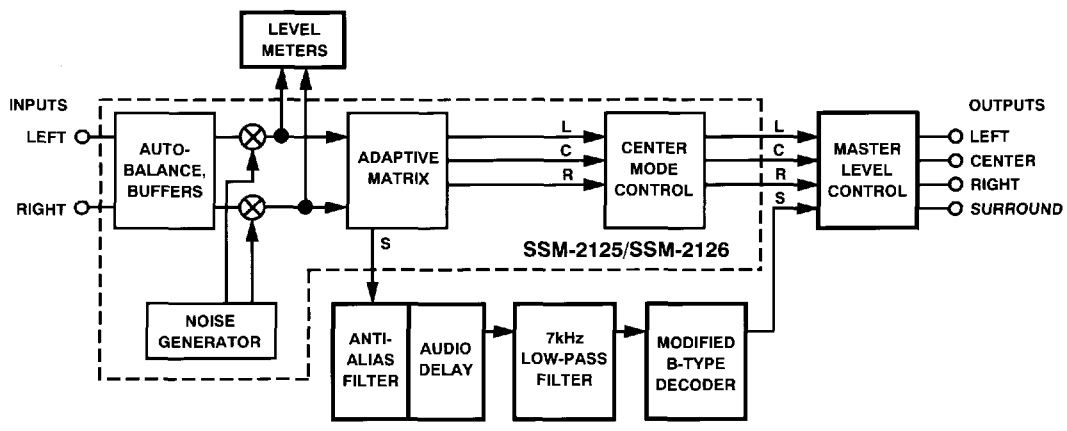
Over 2000 major films and an increasing number of broadcasts are available in Dolby Surround. Surround encoding is preserved in the stereo audio tracks of normal video discs, video cassettes, and television broadcasts, permitting the decoding to multichannel audio in the home.

Major design considerations of the SSM-2125/SSM-2126 are excellent audio performance and a high level of integration. In addition to the Adaptive Matrix and Center Mode Control, also included on-chip are the Automatic Balance Control and Noise Generator functions. A complete Pro-Logic system can be realized using the SSM-2125/SSM-2126 and few external components. Using SSM's extensive experience in the design of professional audio integrated circuits, the SSM-2125/SSM-2126 offers typical 103 dB dynamic range and 0.025% THD. A direct path bypass mode allows normal stereo operation with high fidelity without the need for external switching or parallel signal paths.

The SSM-2125 is a premium grade that is selected to a minimum channel separation specification of 35 dB for the center to left and right channels, and 25 dB for the remaining channels. The standard grade, the SSM-2126, provides minimum channel separation of 25 dB from any channel to another.

The SSM-2125/SSM-2126 is available only to licensees of Dolby Licensing Corporation, San Francisco, California, from whom licensing and application information must be obtained.

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

SSM-2125/SSM-2126—SPECIFICATIONS (V_S = ±6 V, T_A = +25°C, V_{IN} = 0 dBd at 1 kHz,[1] Center Mode Control: Wide, unless otherwise noted.)

Parameter	Symbol	Conditions	SSM-2125 Min	SSM-2125 Typ	SSM-2125 Max	SSM-2126 Min	SSM-2126 Typ	SSM-2126 Max	Units
CHANNEL SEPARATION									
Center		C Input; R, L Outputs	35	48		25	35		dB
		C Input; S Output	25	35		25	35		dB
Right		R Input; L, C, S Outputs	25	35		25	35		dB
Left		L Input; C, R, S Outputs	25	35		25	35		dB
Surround		S Input; L, R, C Outputs	25	35		25	35		dB
CHANNEL OUTPUT LEVEL		V_{IN} = 0 dB; L, R, C, S Output			±0.5			±0.5	dBd
TOTAL HARMONIC DISTORTION	THD	All Channels		0.02	0.1		0.02	0.1	%
SIGNAL-TO-NOISE RATIO	SNR	V_{IN} = 0 V, CCIR2K/ARM All Channels	−83	−87		−80	−87		dBd
HEADROOM	HR	Clipping = 3% THD All Channels	15	16		15	16		dBd
BYPASS MODE DYNAMIC RANGE		Clipping to Noise Floor		104			104		dB
NOISE SOURCE OUTPUT LEVEL		All Channels		−13.5			−13.5		dBd
NOISE SOURCE OUTPUT LEVEL MATCHING		Any Channel to Another		1			1		dB
AUTOBALANCE CAPTURE RANGE			±3	±3.8	±6		±3.8		dB
LOGIC THRESHOLD HI LO		Relative to L_{REF}	+2.4		 +0.8	+2.4		 +0.8	V V
OPERATING SUPPLY VOLTAGE	V_S	Single Supply Dual Supply		+12 ±6			+12 ±6		V V
SUPPLY CURRENT	I_{SY}	No Input Signal		40	50		40	50	mA
INPUT IMPEDANCE	Z_{IN}	L, R Inputs		5			5		kΩ
OUTPUT IMPEDANCE	Z_{OUT}	L, R, C, S Outputs		600			600		Ω

NOTE
[1]0 dBd = 500 mV rms Dolby level output at any channel; Left and Right inputs: 500 mV rms (0 dBd); Center input: L = R = 354 mV rms (−3 dBd); Surround input: L = −R = 354 mV rms (−3 dBd).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +16 V or ±8 V
Logic Inputs . . . . . V+ to V−
Storage Temperature Range . . . . . −55°C to +125°C
Operating Temperature Range . . . . . −20°C to +70°C
Junction Temperature . . . . . +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C
Thermal Resistance[1]
θ_{JA} . . . . . 38°C/W
θ_{JC} . . . . . 14°C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., device in socket.

ORDERING GUIDE

Model	Temperature Range	Package Option
SSM2125XXXP*	−20°C to +70°C	48-Pin P-DIP
SSM2126XXXP*	−20°C to +70°C	48-Pin P-DIP

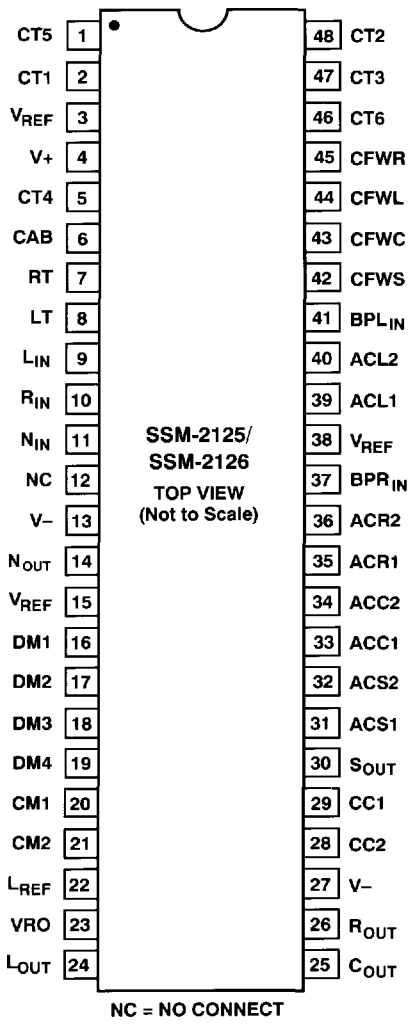
NOTE
*The SSM-2125/SSM-2126 is available only to licensees of Dolby Laboratories. Each customer will be assigned a special part number for ordering purposes. Contact local ADI sales office for further details.

Table I. External Component List

Component	Value	Tolerance*	Comment (Noncritical Unless Otherwise Noted)
C1	0.1 μF		
C2	0.1 μF		
C3	680 pF		
C4	0.1 μF		
C5	0.1 μF		
C6	680 pF		
C7	4.7 μF	20%	Standard Electrolytic
C8	0.22 μF		
C9	0.22 μF		
C10	0.33 μF		Film
C11	0.33 μF		Film
C12	0.33 μF		Film
C13	0.33 μF		Film
C14	22 nF		Film
C15	22 nF		Film
C16	22 nF		Film
C17	22 nF		Film
C18	0.1 μF		
C19	4.7 μF	20%	Standard Electrolytic
C20	0.22 μF		
C21	0.22 μF		
C22	10 μF	20%	Standard Electrolytic
C23	—	—	Not Needed
C24	10 nF		
C25	10 nF		
C26	10 nF		
C27	100 μF	≥100 μF	Standard Electrolytic
C28	0.1 μF		
C29**	100 μF	≥100 μF	Standard Electrolytic
C30**	0.1 μF		
C31	100 μF	≥100 μF	Standard Electrolytic
C32	0.1 μF		
R1	15 kΩ	5%	
R2	47 kΩ	5%	
R3	15 kΩ	5%	
R4	47 kΩ	5%	
R5	7.5 kΩ	5%	
R6	7.5 kΩ	5%	
R7	—	—	Not Needed
R8	—	—	Not Needed
R9	22 kΩ	5%	
R10	22 kΩ	5%	
R11	10 MΩ	5%	
R12	22 kΩ	5%	

NOTES
*10% unless otherwise indicated.
**Used only in Dual Supply Application Circuit.

PIN CONNECTIONS



PIN DESCRIPTION

Pin #	Name	Function
1	CT5	Long Time Constant, C/S
2	CT1	Short Time Constant, L/R Comparators
3	V_{REF}	Reference Voltage: Ground or Pseudoground
4	V+	Positive Supply
5	CT4	Short Time Constant, C/S Comparators
6	CAB	Autobalance Time Constant
7	RT	Buffered, Autobalanced Right Channel Signal
8	LT	Buffered, Autobalanced Left Channel Signal
9	L_{IN}	Left Channel Input
10	R_{IN}	Right Channel Input
11	N_{IN}	Filtered Noise Input
12	NC	Do Not Connect
13	V–	Negative Supply (Ground in Single Supply)
14	N_{OUT}	Noise Output
15	V_{REF}	Reference Voltage: Ground or Pseudoground
16	DM1	Digital Operating-Mode Control Input
17	DM2	Digital Operating-Mode Control Input
18	DM3	Digital Operating-Mode Control Input
19	DM4	Digital Operating-Mode Control Input
20	CM1	Digital Center-Mode Control Input
21	CM2	Digital Center-Mode Control Input
22	L_{REF}	Logic Reference Voltage (Threshold = L_{REF} + 1.4 V)
23	VRO	V_{REF} Out—Pseudoground Output
24	L_{OUT}	Left Channel Output
25	C_{OUT}	Center Channel Output
26	R_{OUT}	Right Channel Output
27	V–	Negative Supply (Ground in Single Supply)
28	CC2	Center Normal-Mode Filter Input (Z = 15 kΩ)
29	CC1	Center Normal-Mode Filter Output
30	S_{OUT}	Surround Channel Output
31	ACS1	Surround Channel Steering Signal AC Coupling and High-Pass Filter
32	ACS2	Surround Channel Steering Signal AC Coupling and High-Pass Filter
33	ACC1	Center Channel Steering Signal AC Coupling and High-Pass Filter
34	ACC2	Center Channel Steering Signal AC Coupling and High-Pass Filter
35	ACR1	Right Channel Steering Signal AC Coupling and High-Pass Filter
36	ACR2	Right Channel Steering Signal AC Coupling and High-Pass Filter
37	BPR_{IN}	Filtered Right Channel Input to Steering Signal Generator
38	V_{REF}	Reference Voltage: Ground or Pseudoground
39	ACL1	Left Channel Steering Signal AC Coupling and High-Pass Filter
40	ACL2	Left Channel Steering Signal AC Coupling and High-Pass Filter
41	BPL_{IN}	Filtered Left Channel Input to Steering Signal Generator
42	CFWS	Surround Channel Full-Wave Rectifier Low-Pass Filter
43	CFWC	Center Channel Full-Wave Rectifier Low-Pass Filter
44	CFWL	Left Channel Full-Wave Rectifier Low-Pass Filter
45	CFWR	Right Channel Full-Wave Rectifier Low-Pass Filter
46	CT6	Short Time Constant, C/S
47	CT3	Short Time Constant, L/R
48	CT2	Long Time Constant, L/R

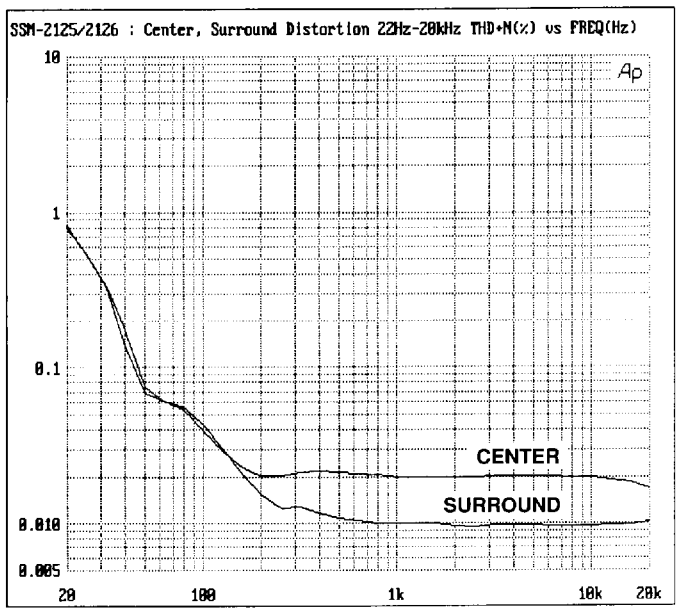


Figure 1. THD+N vs. Frequency, Center and Surround Channels (V_{IN} = 0 dBd, R_L = 100 kΩ)*

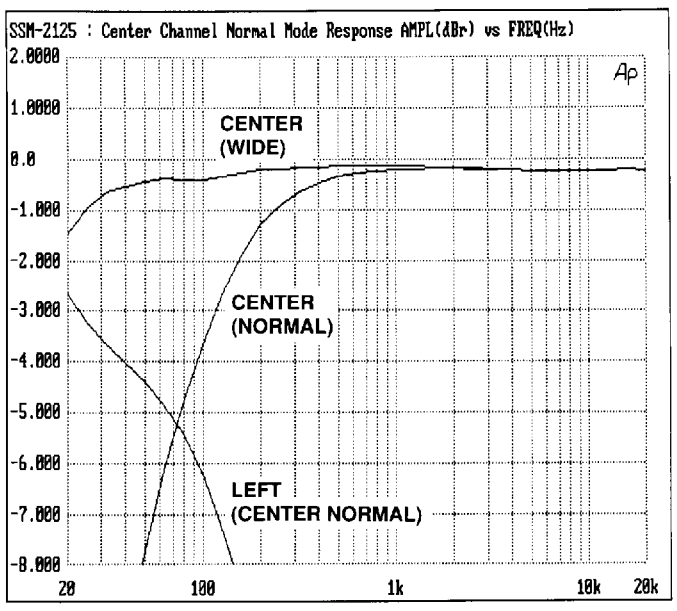


Figure 3. Bass-Splitting Filter Response (Center Channel Normal and Wide Modes)

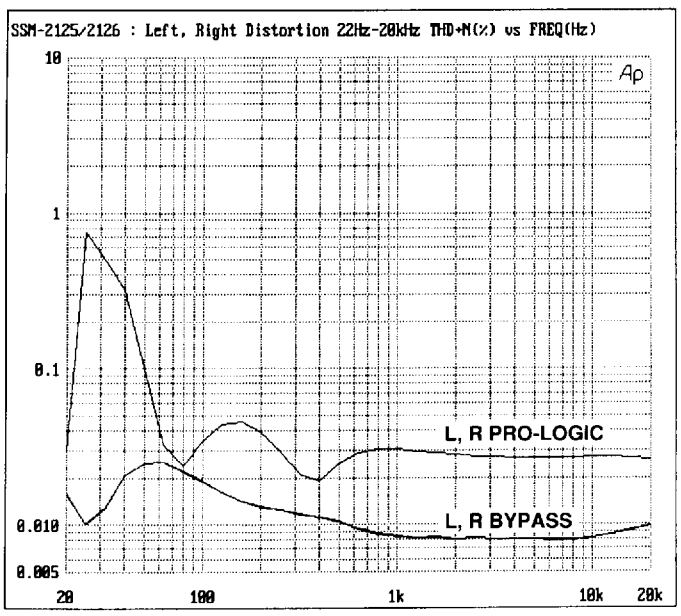


Figure 2. THD+N vs. Frequency, Left and Right Channels (V_{IN} = 0 dBd, R_L = 100 kΩ)*

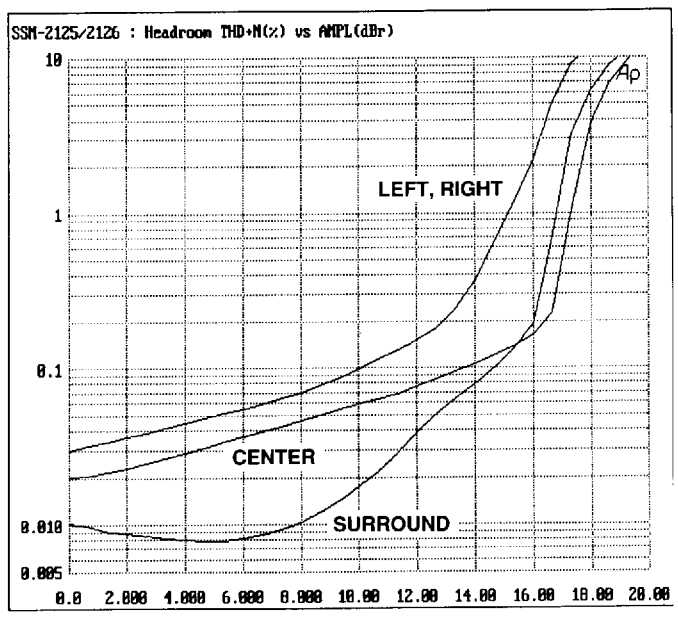


Figure 4. Headroom THD+N vs. Amplitude (0 dBr = 0 dBd = 500 mV rms)

*80 kHz low-pass filter used for Figures 1 and 2.

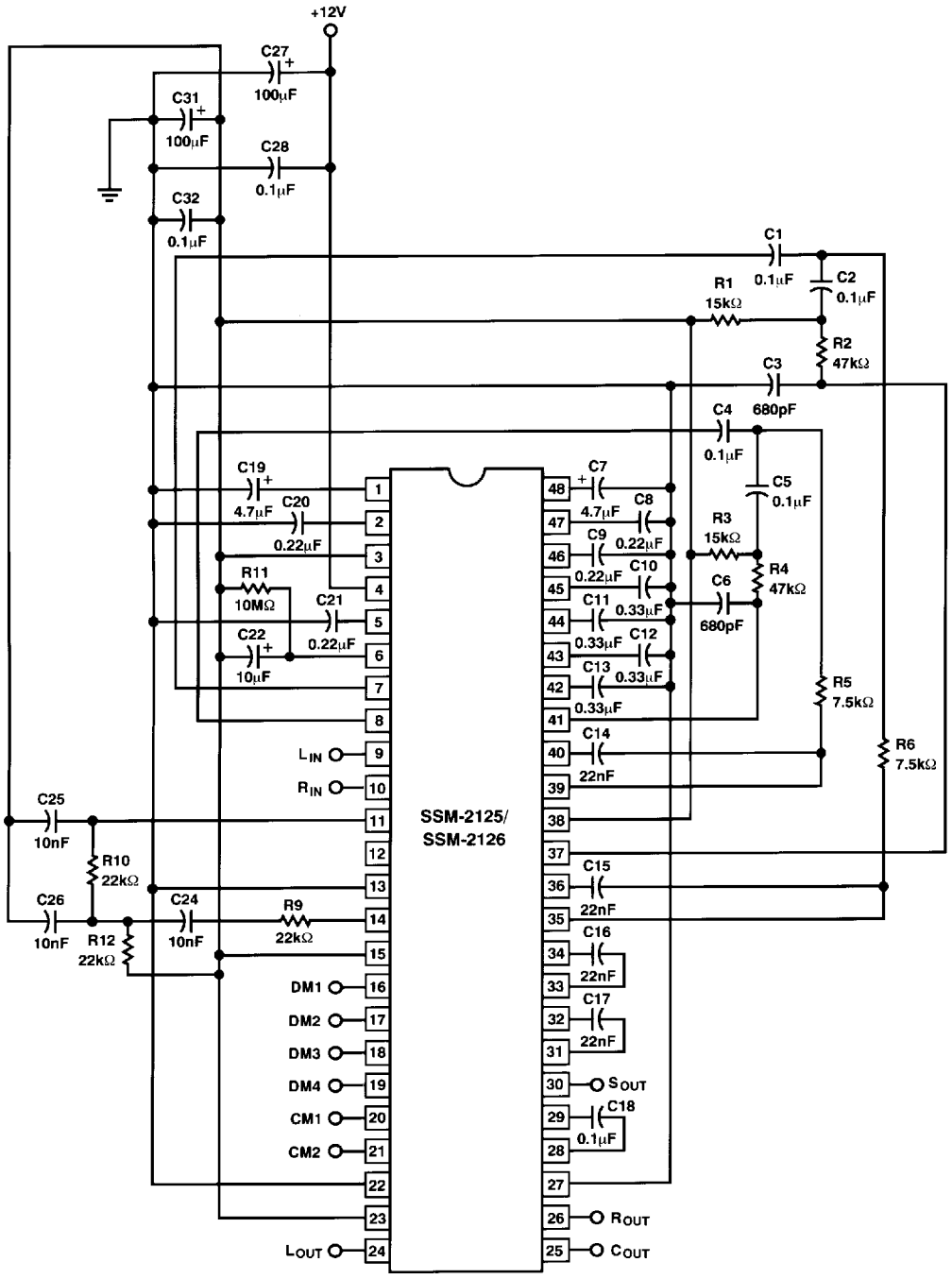


Figure 5. Single Supply Application Circuit

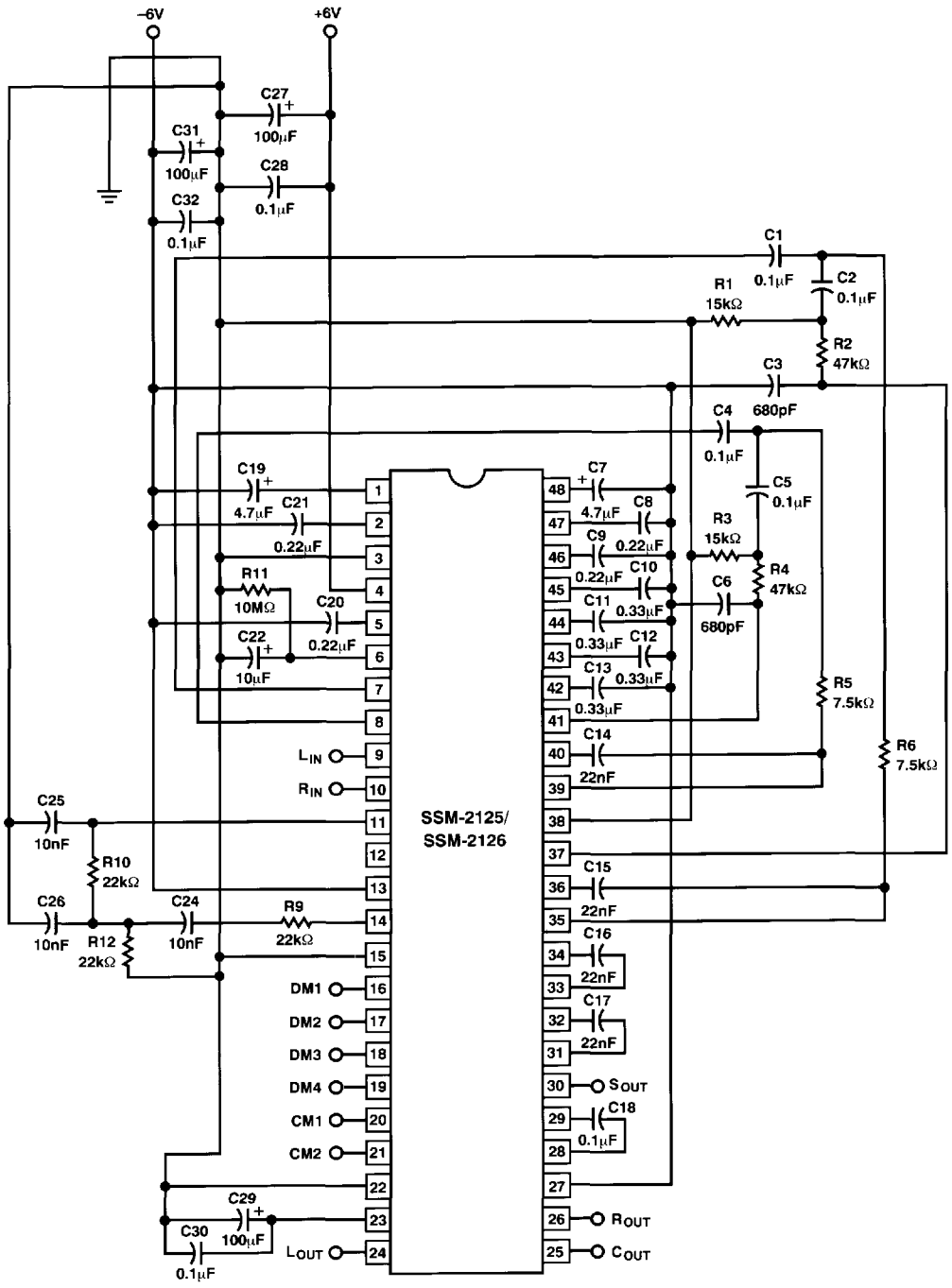


Figure 6. Dual Supply Application Circuit

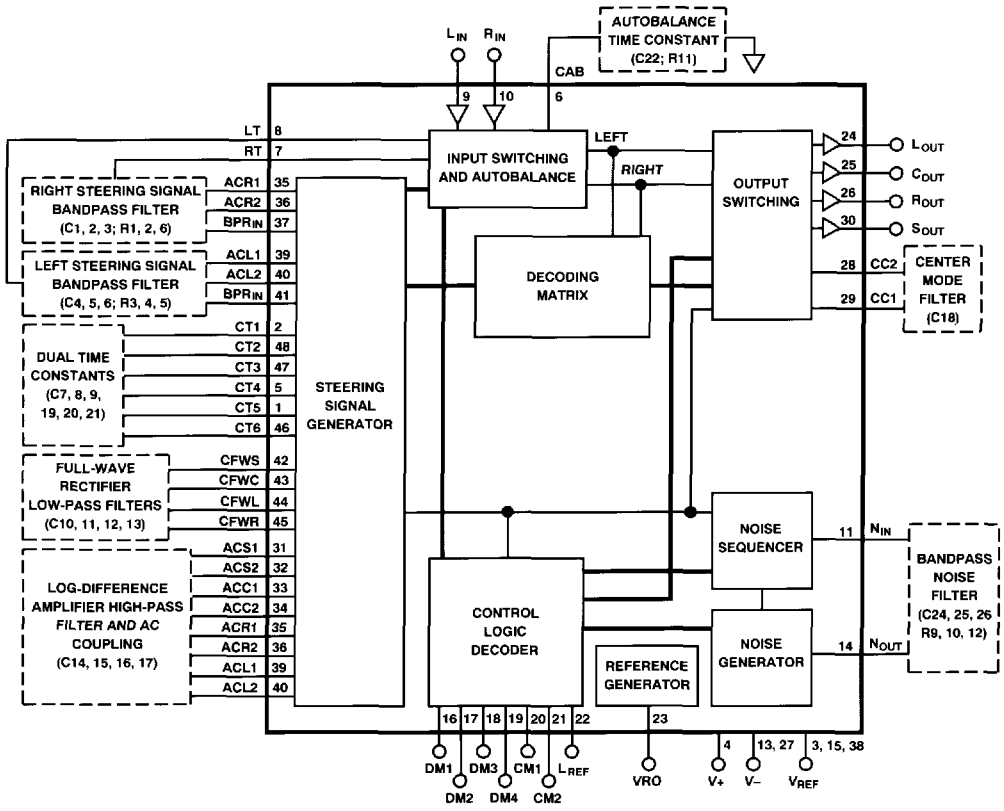


Figure 7. SSM-2125/SSM-2126 Block Diagram Showing External Component Functions

APPLICATIONS INFORMATION

POWER SUPPLIES

The SSM-2125/SSM-2126 is designed to use either a dual ±6 V or single +12 V supply, with a tolerance of ±10%. Internal reference points on the IC and a 6 V reference, generated on-chip, are brought to external pins. When operated in dual supply mode, the reference inputs (labeled V_{REF}) are connected to the external ground. In single supply mode, the internal 6 V reference (labeled VRO) is wired to the V_{REF} pins, providing a pseudoground reference. In either mode, the internal reference VRO should be decoupled with a 100 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.

Dual supply mode offers the highest fidelity operation and eliminates the necessity for input and output decoupling capacitors. All signals are ground referenced in dual supply mode, allowing dc coupling of the inputs and outputs. Additionally, the power on settling time is reduced when operating with dual supplies.

In single supply mode, decoupling capacitors are required, as the signals are referenced to the +6 V pseudoground reference. Any noise introduced onto the V_{REF} line will appear at the output, so careful decoupling of the reference is required to maintain excellent noise and distortion performance. The 100 µF V_{REF} decoupling capacitors should be placed close to the VRO pin (Pin 23), and 0.1 µF capacitors close to each V_{REF} pin.

DOLBY LEVEL

The discrete implementation of Dolby Pro-Logic Surround used a Dolby level of 500 mV. To maintain high audio quality and excellent signal-to-noise ratio, the SSM-2125/SSM-2126 was designed to operate with a 500 mV Dolby level. With this level, the SSM-2125/SSM-2126 provides 87 dBd SNR (CCIR2K/ARM) and 16 dB of headroom. In addition, the SSM-2125/SSM-2126 is capable of operation to the Pro-Logic specification at a Dolby level of 300 mV, with the result of reduced SNR and increased headroom. At the 300 mV level, SNR is typically 83 dBd with 20 dB of headroom. Either way, total dynamic range of the device is 103 dB (0 dBd = 500 mV).

AUTOBALANCE

Left and right signals with an imbalance less than ±3.8 dB will activate the autobalance circuitry when DM3 = 1. Once activated, the circuit will correct up to 4 dB of balance error. Autobalance is available in both the Pro-Logic and stereo bypass modes. When autobalance is OFF, the autobalance VCAs are bypassed.

NOISE GENERATOR AND SEQUENCING

The SSM-2125/SSM-2126 noise source is best described as white noise passed through a 0.2 Hz comb filter and a 10 kHz low-pass filter. Thus, the noise is comprised of separate equal-amplitude peaks spaced at 0.2 Hz apart, as shown in Figure 8. Figure 9 shows overall frequency response of the filtered noise source.

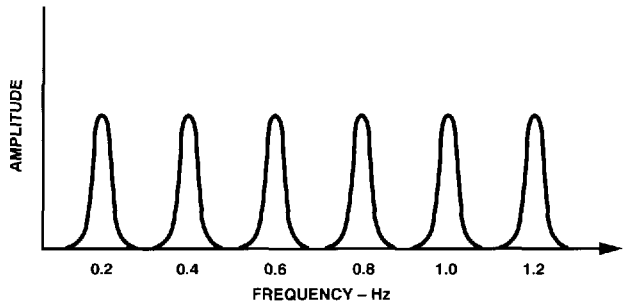


Figure 8. Comb-Filtered Noise Source Characteristics

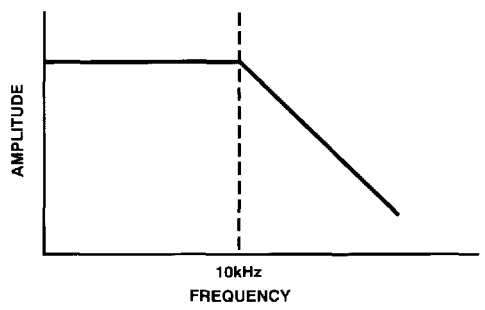


Figure 9. Overall Frequency Response of Filtered Noise Source

For systems that are not microprocessor controlled, Figure 10 suggests one option to implement automatic noise sequencing using standard logic. The CD4060 (or equivalent), although only partially used, was selected since it contains a clock and 2-bit binary counter on-chip. The timing interval is set by:

$$f = \frac{1}{2.2\ R_1\ C_3}$$

where $2R_1 < R_2 < 10R_1$.

The values shown in Figure 10 will provide a frequency of 2.9 Hz. One half of a CD4556 can be used to drive LED panel indicators if desired, as shown.

FUNCTIONAL MODES

The SSM-2125/SSM-2126 uses a positive logic system, whereby a voltage greater than 2.4 V above L_{REF} is considered a "1," and voltage levels between L_{REF} and 0.8 V are considered a "0." Tables II and III provide truth tables for logic inputs DM1 through DM4, and CM1 and CM2. "Dolby 3" mode, which disables surround steering, is available as shown. Normal operating mode for the decoder is with a "1" on all logic inputs. This provides 4-channel logic, autobalance ON, and center normal mode. Internal pullups will automatically set the chip into this state if the inputs are left unconnected.

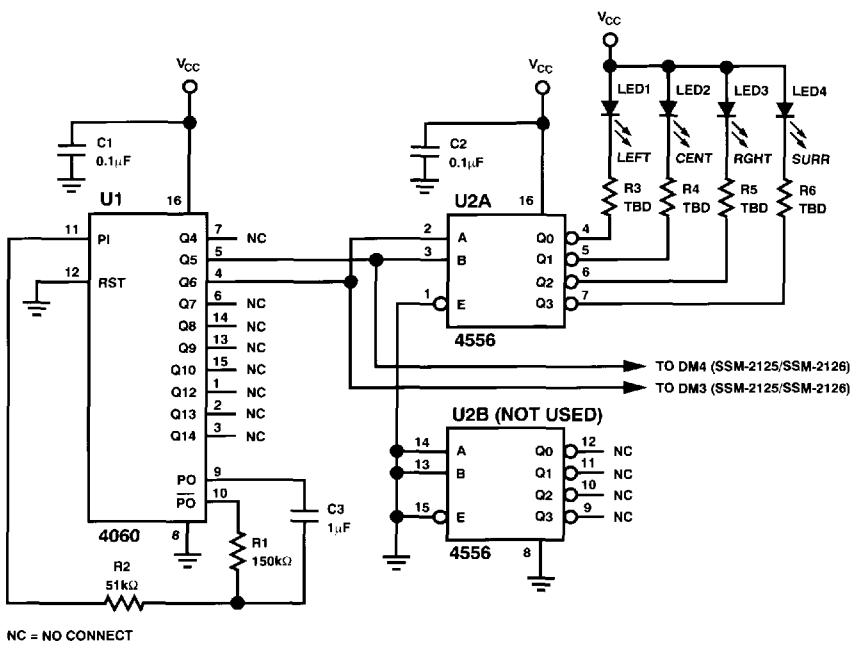


Figure 10. Automatic Noise Sequencing Circuit

Table II. Control States for DM1–DM4

DM1	DM2	DM3	DM4	Operating State
1	1	1	1	Dolby 4-Channel ("Pro-Logic"), Autobalance On
1	1	0	1	Dolby 4-Channel ("Pro-Logic"), Autobalance Off
1	0	1	1	Dolby 3-Channel ("Dolby 3"), Autobalance On
1	0	0	1	Dolby 3-Channel ("Dolby 3"), Autobalance Off
0	1	1	1	Surround Channel Noise
0	1	1	0	Right Channel Noise
0	1	0	1	Center Channel Noise
0	1	0	0	Left Channel Noise
0	0	X	1	Mute
0	0	1	0	Stereo Bypass, Autobalance On
0	0	0	0	Stereo Bypass, Autobalance Off

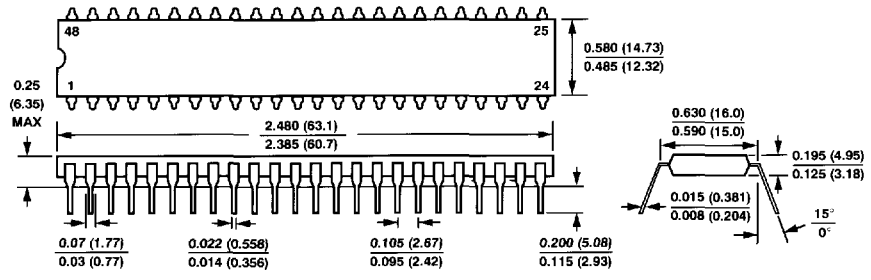
Table III. Center Channel Functional Modes

CM1	CM2	Mode
0	0	Center Channel Off
0	1	Center Channel Wideband
1	0	Phantom Center Channel
1	1	Normal Center Mode

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Pin Plastic DIP



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