PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8630 A, B&M
600MHz DECADE COUNTER
SP8631A, B&M
500MHz DECADE COUNTER
SP8632 A, B&M
400MHz DECADE COUNTER

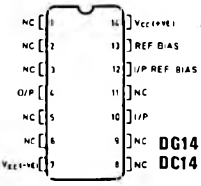
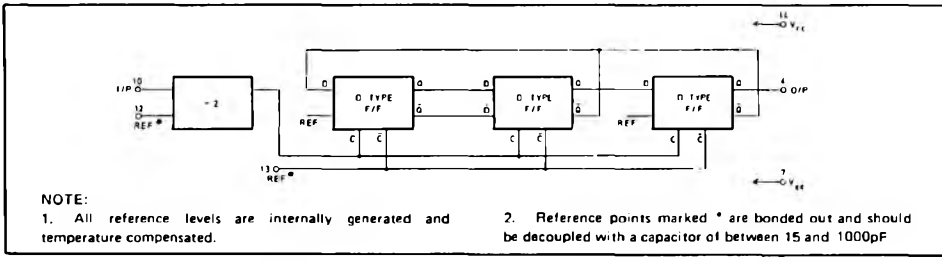


Fig. 1 Pin connections

GENERAL DESCRIPTION

The SP8630/1/2 counters are fixed ratio ÷ 10 circuits using emitter coupled logic, with maximum specified counting frequencies of 600, 500 and 400 MHz respectively, over temperature ranges of −55°C to +125°C, 0°C to 70°C and −40°C to +85°C. A 6:4 mark/space square wave is provided at the emitter follower output. The input is normally single driven and capacitively coupled to the signal source. There are two bias points on the circuit which should be capacitively coupled to the ground plane.



NOTE:
1. All reference levels are internally generated and temperature compensated.
2. Reference points marked * are bonded out and should be decoupled with a capacitor of between 15 and 1000pF

Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless stated otherwise):

Tamb: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'C' grade −40°C to +85°C

Operating supply voltage
V_{CC} 0V
V_{EE} −5.2V ± 0.25V
Input voltage 400 to 800 mV (p-p)
Output load 500Ω & 3pF.

NOTE: The maximum input frequency is guaranteed at V_{EE} = −5.2V. For typical operating characteristics with power supply variations see Fig.5, which shows that the maximum operating frequency of a typical device increases with increasing power supply voltage

Characteristic	Type	Value			Units	Conditions
		Min	Typ	Max		
Max input freq.	SP8630	600			MHz	
	SP8631	500			MHz	
	SP8632	400			MHz	
Min input freq. with sinusoidal input	All		20	40	MHz	
Min. slew rate of square wave I/P for correct operation	All		30	100	V/μs	
Output voltage swing	All	400	600		mV	V_{EE} = −5.2V
Power supply drain current			70		mA	V_{EE} = −5.2V

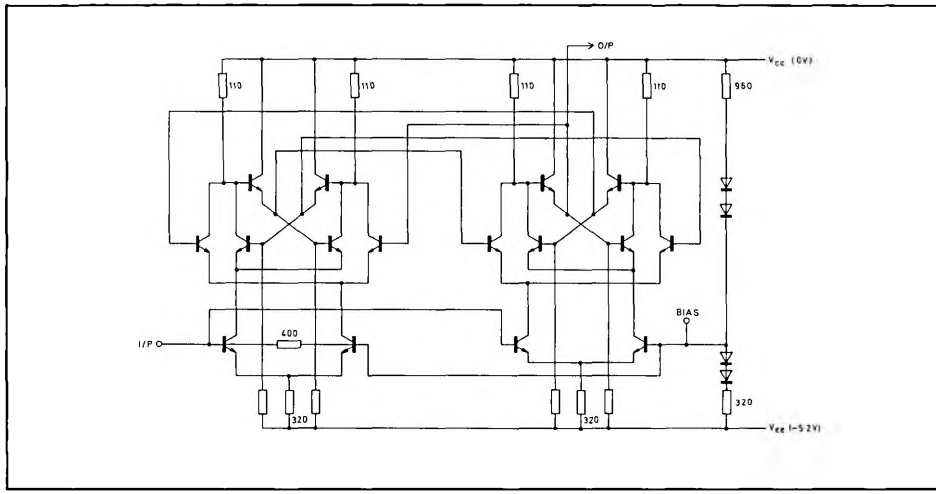


Fig. 3 Circuit diagram of 1st element (–2) showing input biasing arrangement

OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the emitter follower outputs are inadvertantly shorted to ground.

The signal source is normally capacitively coupled to the input: 1000 pF is usually sufficient. If the input signal is likely to be interrupted a 15 k ohm resistor should be connected between the input pin and the negative rail to prevent circuit oscillation under no-signal conditions. The addition of the pulldown resistor causes a slight loss of sensitivity of the device, but this does not normally cause problems in practice.

The input waveform may be sinusoidal, but below 40 MHz the operation of the circuit becomes dependent on the slew rate of the waveform rather than the amplitude. A square wave input with a slew rate of 100 V/μs will allow correct operation down to DC. At high frequencies, increasing drive level above minimum typically increases the max. operating frequency by up to 25%

The output swing of the device can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5k ohms will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8630 series devices to drive directly into ECL II devices with no loss in noise immunity.

The value of capacitance needed for the decoupling capacitors is not critical. Values down to 15 pF have been found satisfactory in practice.

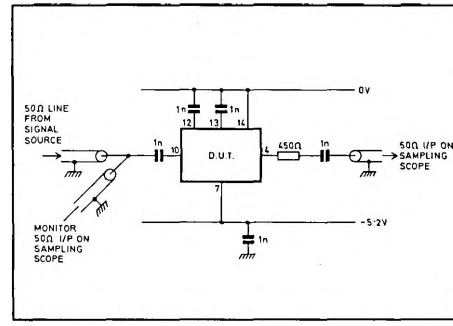


Fig. 4 Test circuit

Test Circuit Notes

The values of the coupling and decoupling capacitors are uncritical but they should be of a type and value suitable for the frequencies involved.

All connections should be physically short when not in a 50Ω environment to minimise reflections due to mismatching.

The +ve pin should be connected to a low impedance earth plane to minimise feed-through of the input signal to the output.

Typical Operating Characteristics

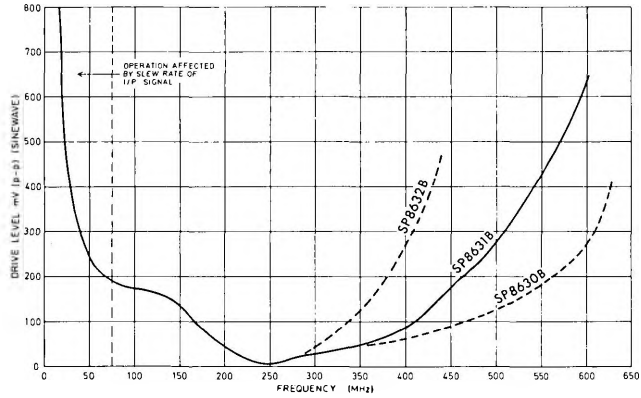


Fig. 5 Minimum drive level v. input frequency at +25 C

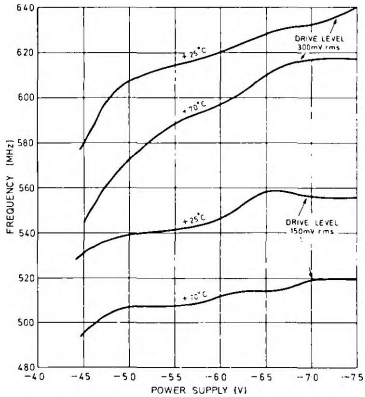


Fig. 6 Max. operating frequency v. power supply voltage for a typical SP8631B

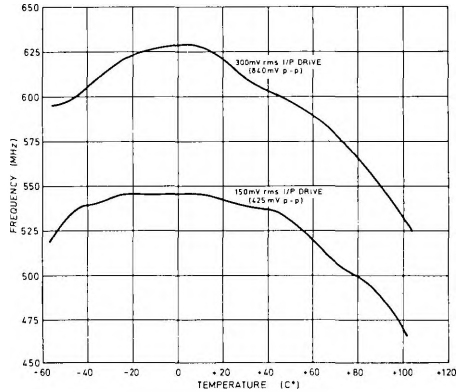


Fig. 7 Max. operating frequency v. ambient temperature for a typical SP8631B (Vcc = −5.2V)

APPLICATION NOTES

Direct coupling to the SP8630 series.

It can be seen from the circuit diagram that the input arrangement of the SP8630 series is not compatible with the normal ECL logic levels. The input reference level is approximately −3.2 volts but it is not well defined and has a temperature coefficient of approximately −1.6 mV/°C. If DC coupling is required, the input would have to be larger than would be the case with capacitive coupling.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	8V.
Input voltage V_{IN}	Not greater than the supply voltage in use
Output current I_{OUT}	15 mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C