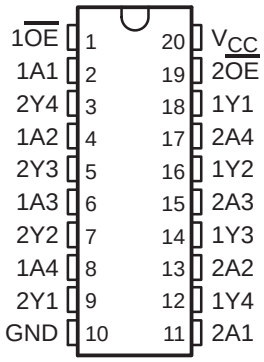
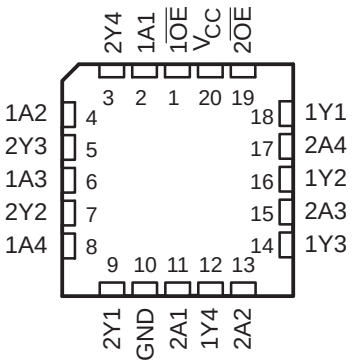
- **Open-Collector Version of ′BCT244**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015**
- **Packages Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (J, N)**

SN54BCT760 . . . J OR W PACKAGE
SN74BCT760 . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT760 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

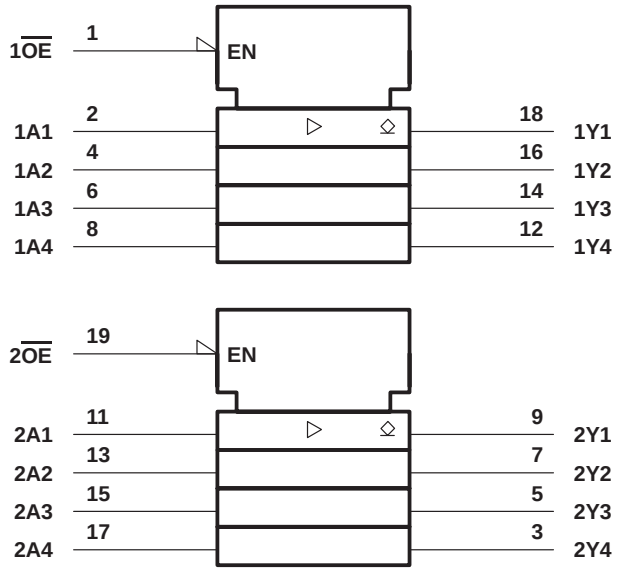
The ′BCT760 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54BCT760 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT760 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each buffer)

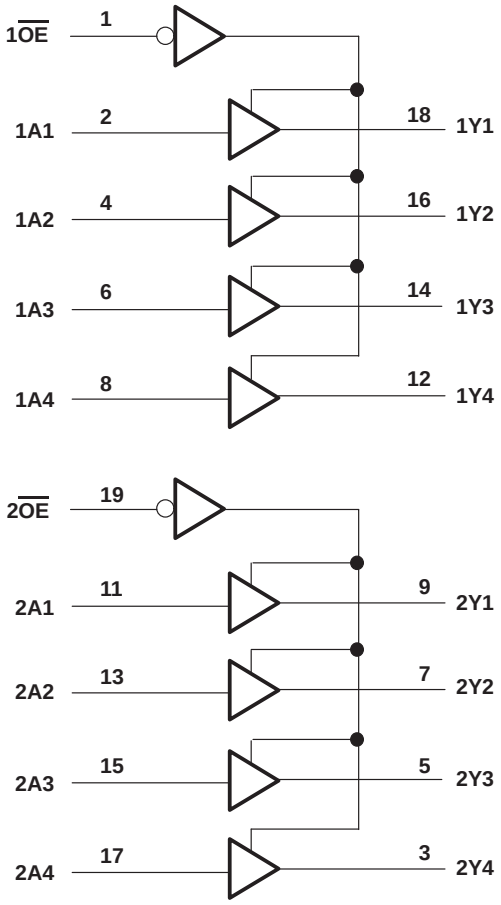
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to 7 V
Input current range, I_I . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Current into any output in the low state: SN54BCT760 . . . . . 96 mA
SN74BCT760 . . . . . 128 mA
Operating free-air temperature range: SN54BCT760 . . . . . – 55°C to 125°C
SN74BCT760 . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The negative input voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT760			SN74BCT760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54BCT760			SN74BCT760			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.38	0.55				V
		I_{OL} = 64 mA						0.42	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V				–1			–1	mA
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V				0.1			0.1	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs open	Outputs high		21	33		21	33	mA
			Outputs low		48	76		48	76	
			$\overline{OE}$ disabled		6	10		6	10	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			6			6		pF
C_o	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			10			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
			′BCT760			SN54BCT760		SN74BCT760		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any A	Y	6.3	8	9.5	6.3	11.1	6.3	10	ns
t_{PHL}			2.1	4.3	6.5	2.1	7.7	2.1	7.2	
t_{PLH}	$\overline{OE}$	Y	8.6	13	15.2	8.6	18.7	8.6	17.5	ns
t_{PHL}			3.2	6.2	8.9	3.2	10.4	3.2	9.9	

‡ For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-9093801M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9093801MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9093801MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN54BCT760J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74BCT760DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74BCT760NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74BCT760NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74BCT760NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54BCT760FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54BCT760J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54BCT760W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF SN54BCT760, SN74BCT760 :

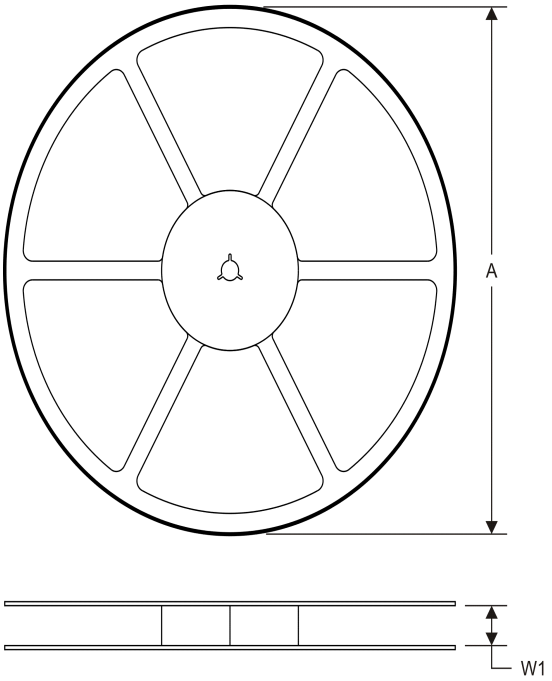
- Catalog: SN74BCT760
- Enhanced Product: SN74BCT760-EP, SN74BCT760-EP
- Military: SN54BCT760

NOTE: Qualified Version Definitions:

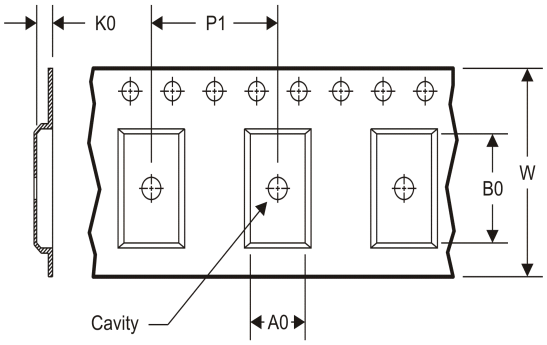
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



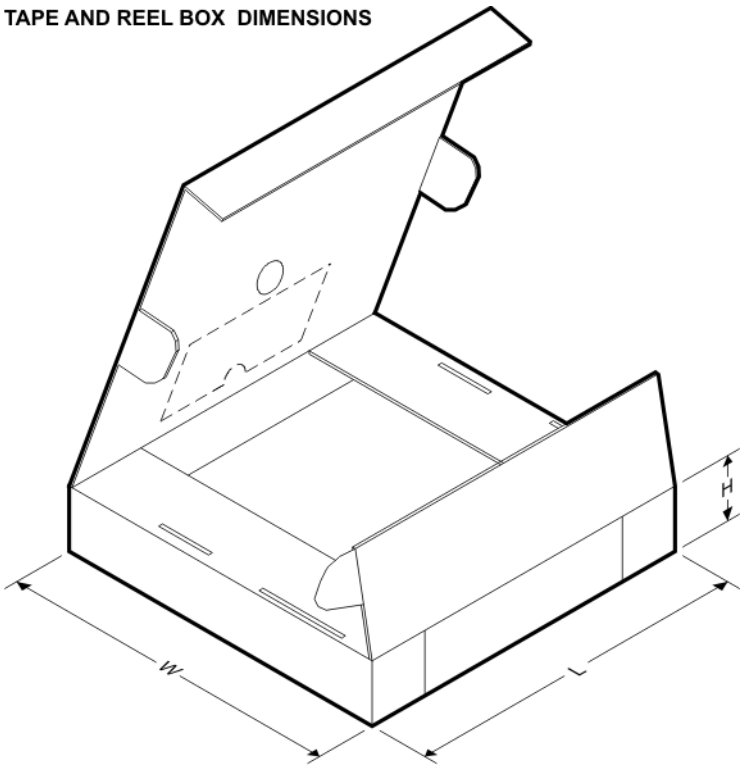
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT760DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74BCT760NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



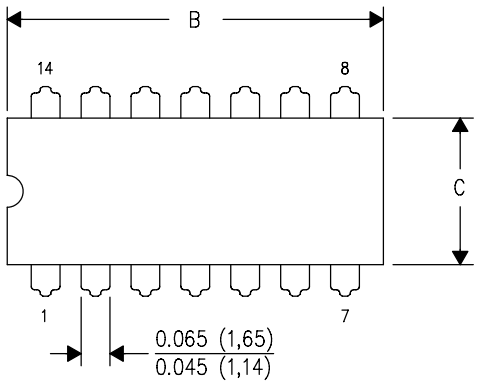
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT760DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74BCT760NSR	SO	NS	20	2000	367.0	367.0	45.0

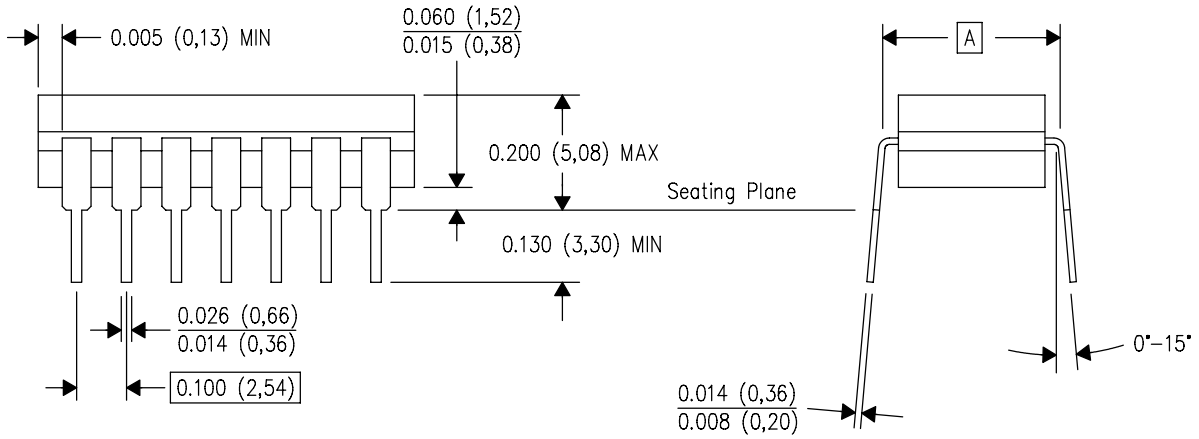
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



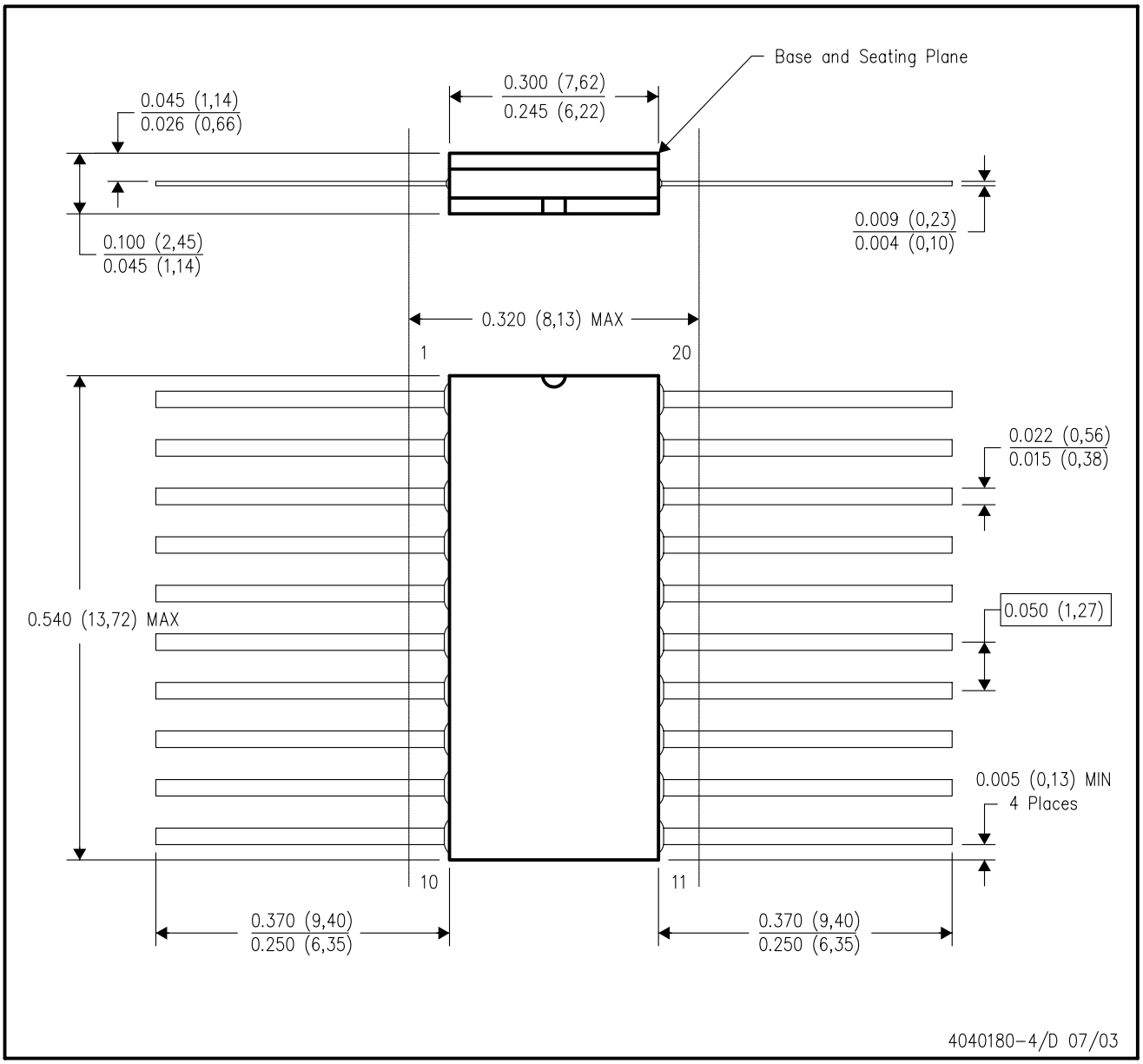
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

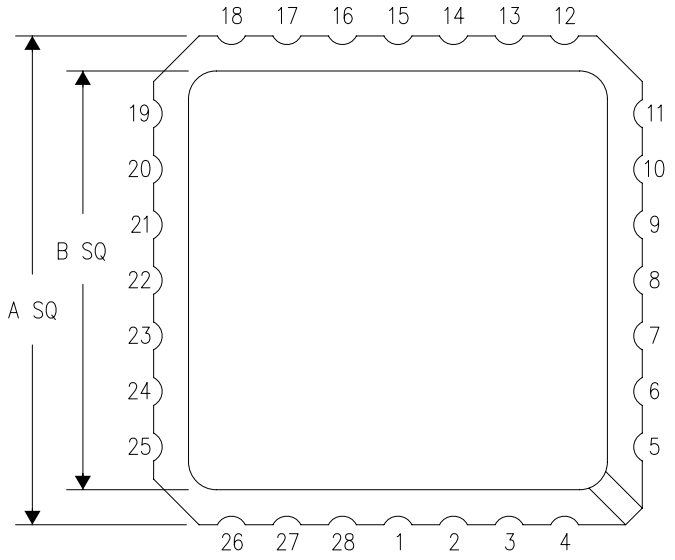
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



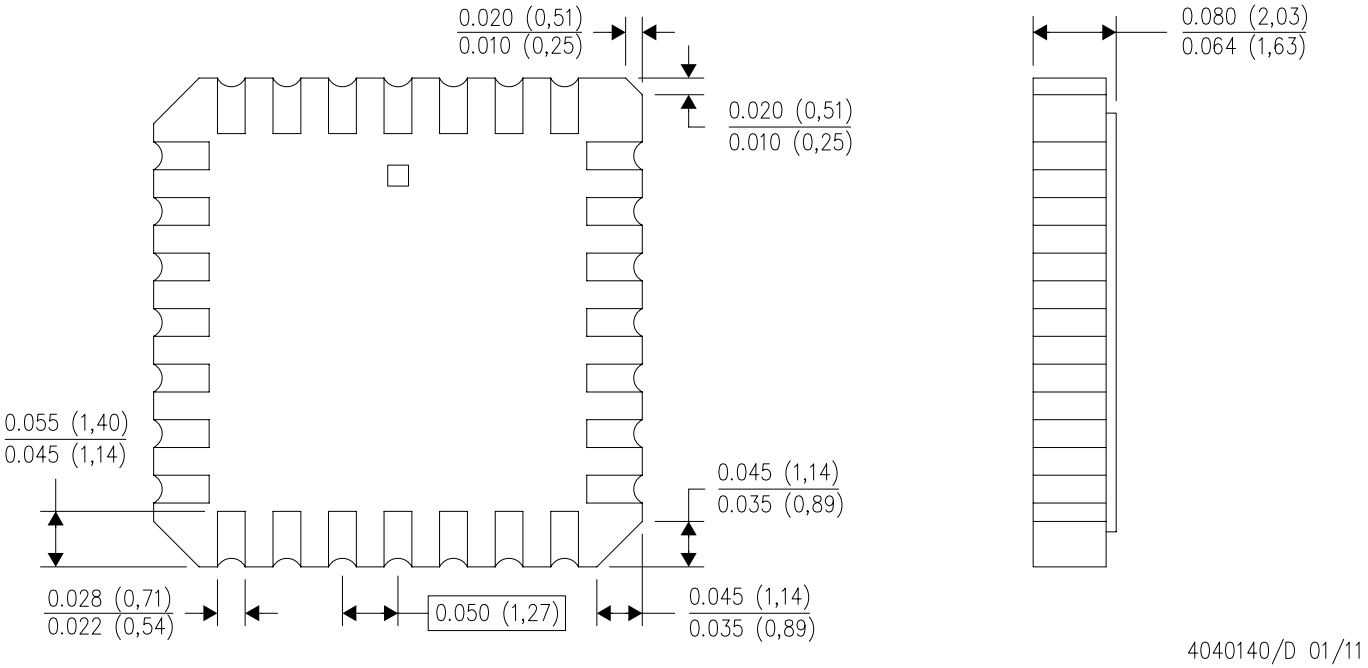
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



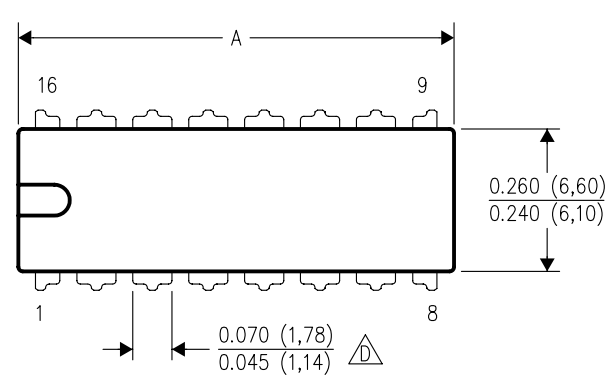
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

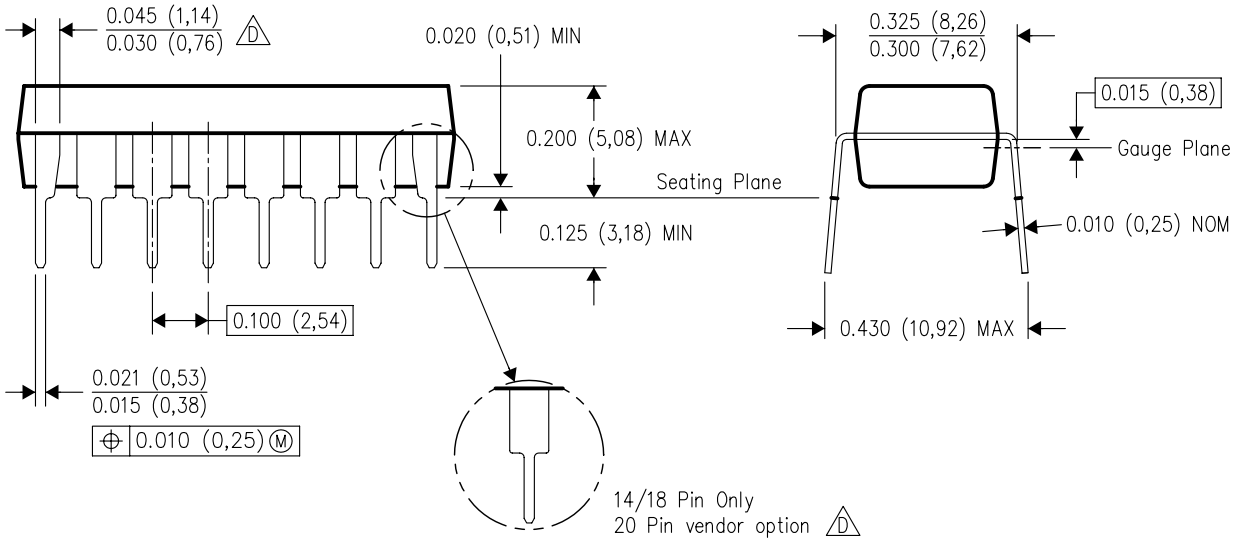
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



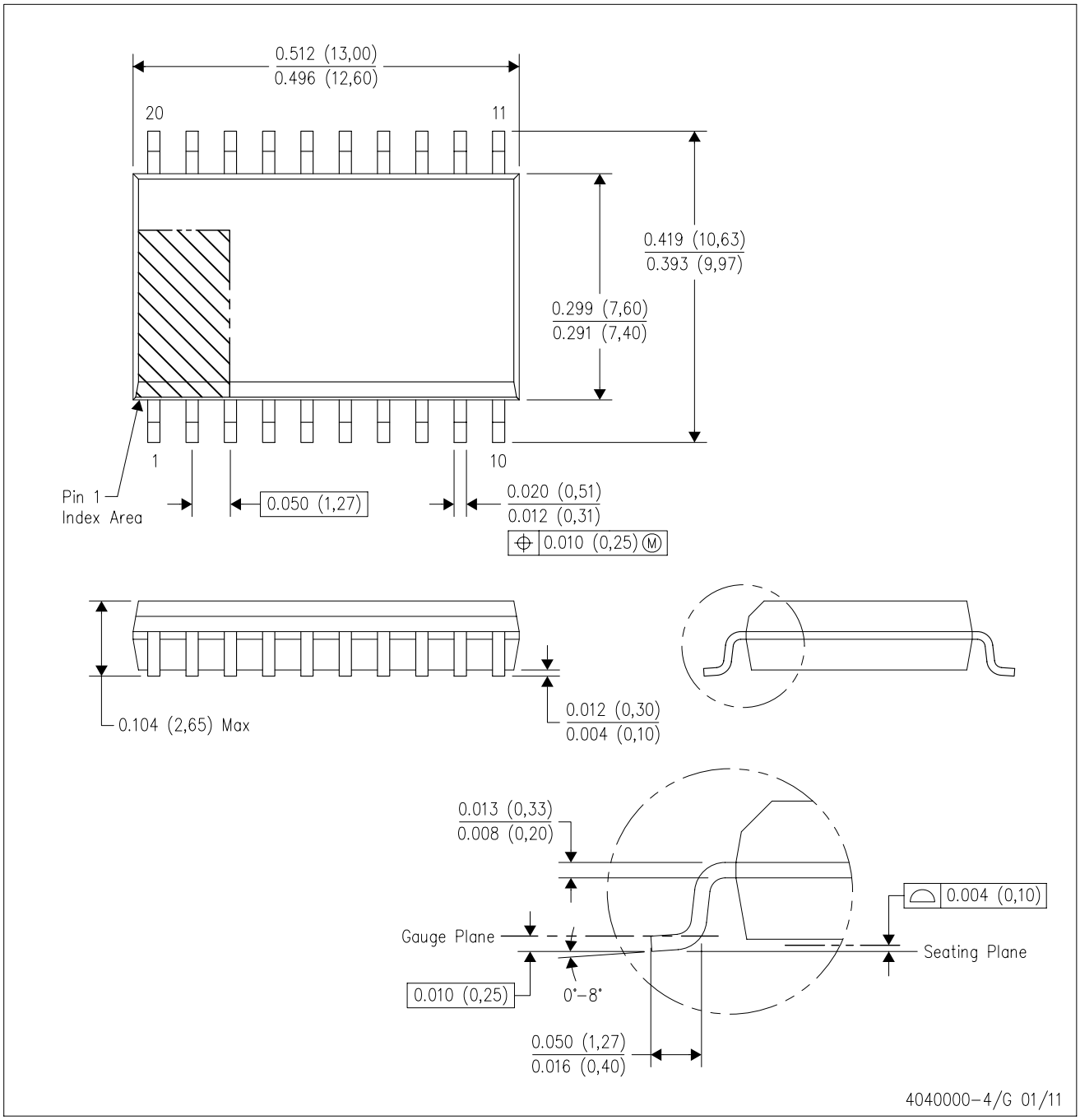
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

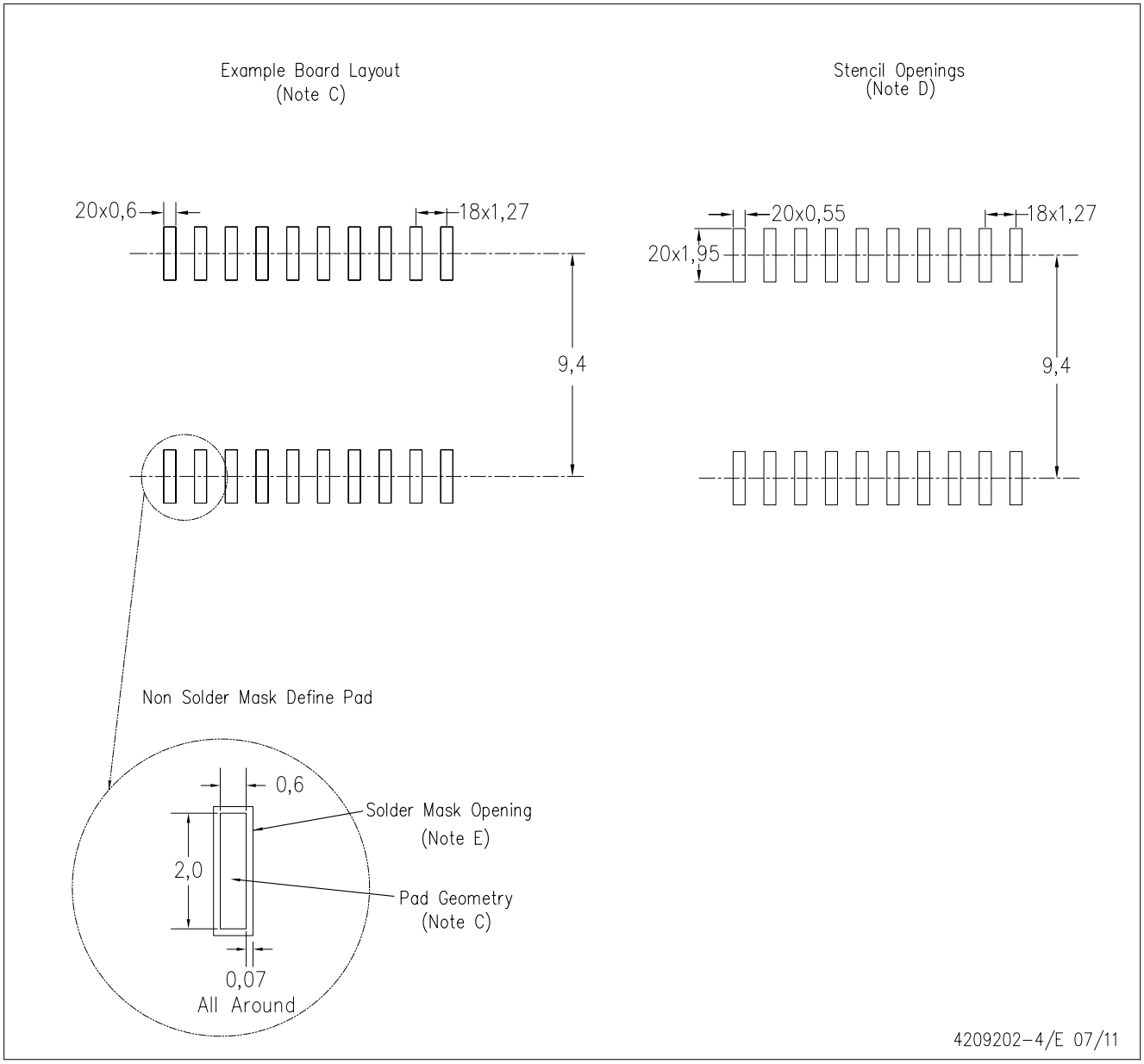
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE

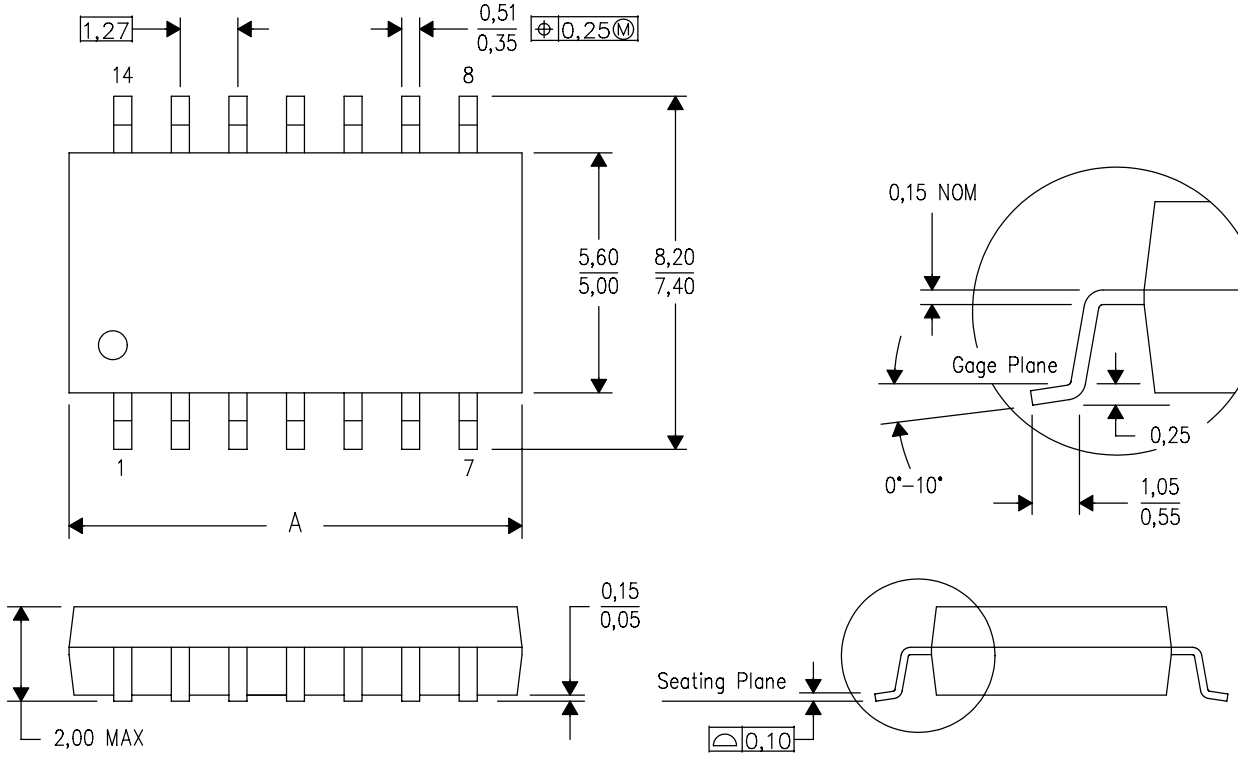


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
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