DATA SHEET

SAA5355
Single-chip colour CRT controller (FTFROM)

Product specification
File under Integrated Circuits, IC02

March 1986

Philips
Semiconductors

PHILIPS

Single-chip colour CRT controller (FTFROM)

SAA5355

GENERAL DESCRIPTION

The SAA5355 FTFROM (Five-Two-Five-ROM) is a single-chip VLSI NMOS crt controller capable of handling the display functions required for a 525-line, level-3 videotex decoder. Only minimal hardware is required to produce a videotex terminal using FTFROM — the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- 32 on-screen colours redefinable from a palette of 4096
- Three on-chip digital-to-analogue converters which compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. FTFROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

  stand-alone built-in oscillator operating with an external 6,041957 MHz crystal

  simple slave directly synchronized from the source of text composite sync

  phase-locked slave indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)
- On-chip timing with composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129); SOT 129-1; 1996 November 18.

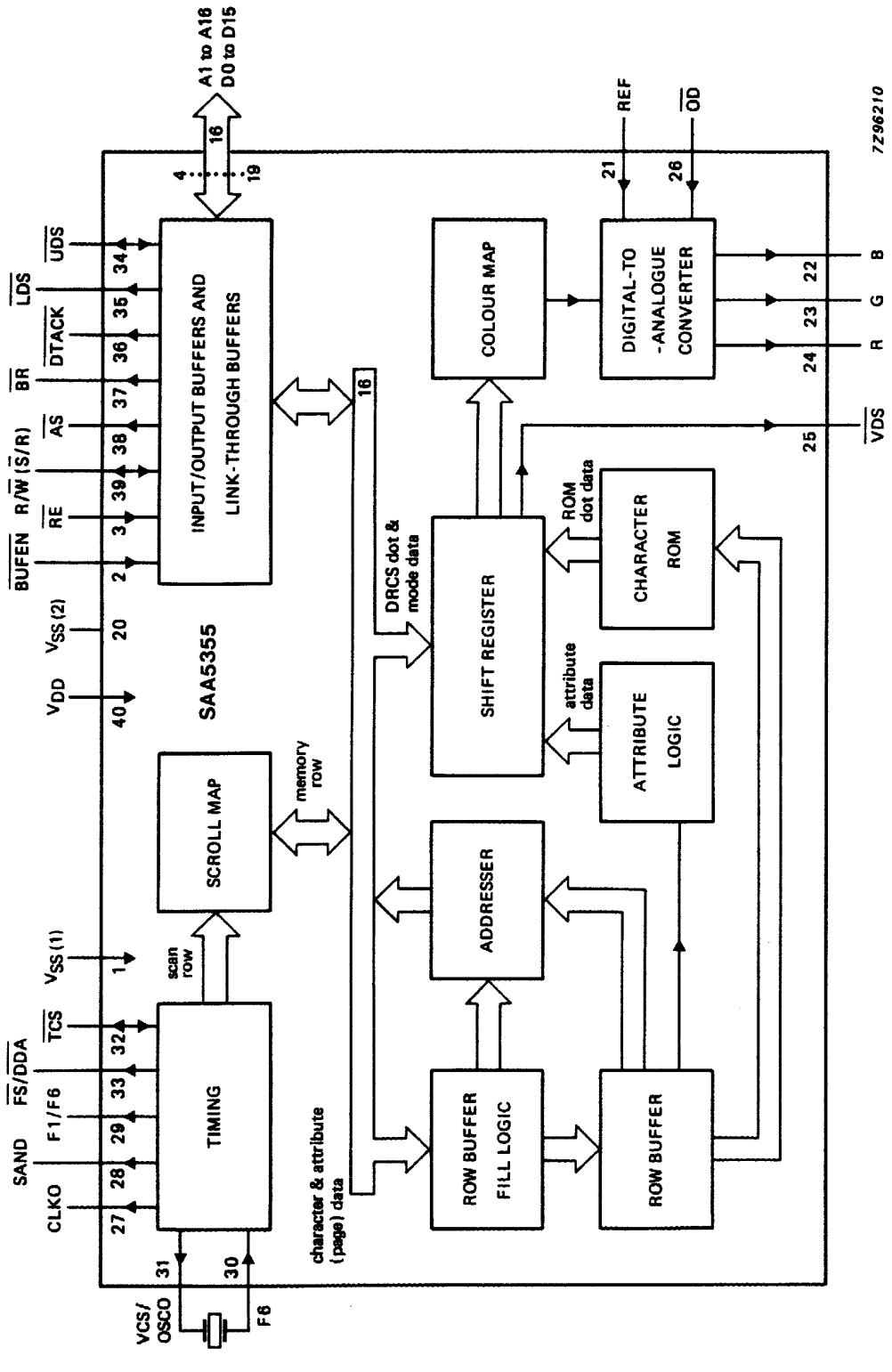


Fig.1 Block diagram.

PINNING

1	$V_{SS(1)}$	Ground (0 V).
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	$V_{SS(2)}$	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3563, TDA3562A).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1,00699 MHz or 6,041957 MHz output.
30	F6	6,041957 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

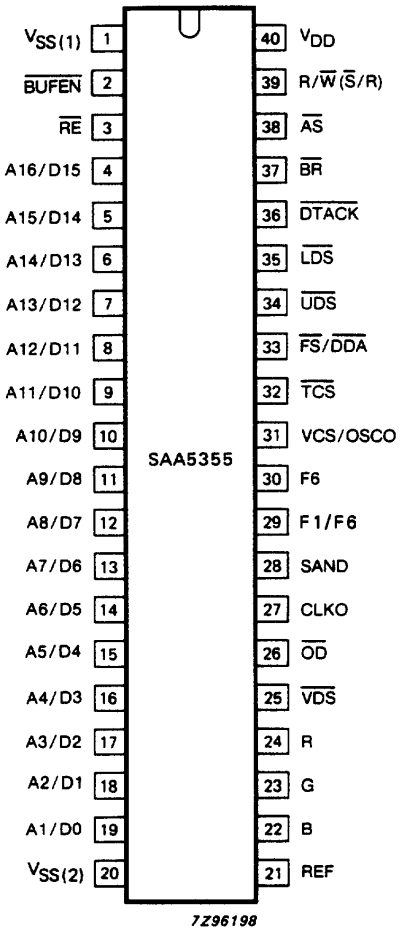


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	–0,3 to + 7,5	V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	–0,3 to + 7,5	V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	–0,3 to + 10,0	V
Maximum input voltage (REF)	V_{REF}	–0,3 to + 3,0	V
Maximum output voltage	V_{Omax}	–0,3 to + 7,5	V
Maximum output current	I_{Omax}	10	mA
Operating ambient temperature range	T_{amb}	–20 to + 70	°C
Storage temperature range	T_{stg}	–55 to + 125	°C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig.3)					
Input voltage (peak-to-peak value)	$V_{I\ (p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	µA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig.4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	note 2	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_I	–10	–	+10	µA
Input capacitance	C_I	–	–	7	pF
REF (Fig.5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 µA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to +10 µA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_{OH} = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	130	pF

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
F1/F6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at					
I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at					
I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 3)					
Output voltage HIGH (note 4) at					
I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state)					
at V_I = 0 to V_{DD} + 0,3 V;					
T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA
$\overline{\text{VDS}}$					
Output voltage HIGH at I_{OH} = −250 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0,4	V
Output voltage LOW at I_{OL} = 1 mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state)					
at V_I = 0 to V_{DD} + 0,3 V;					
T_{amb} = 25 °C	I_{OFF}	−10	–	+10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at					
V_I = 0 to V_{DD} + 0,3 V;					
T_{amb} = 25 °C	I_I	−10	–	+10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance	C_L	–	–	50	pF

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
$\overline{\text{TCS}}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at					
V_I = 0 to V_{DD} + 0,3 V;					
T_{amb} = 25 °C	I_I	–10	–	+10	µA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at					
I_{OH} = –200 to 100 µA	V_{OH}	2,4	–	6,0	V
Output voltage LOW at V_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{\text{UDS}}$, R/$\overline{\text{W}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at					
V_I = 0 to V_{DD}+ 0,3 V;					
T_{amb} = 25 °C	I_I	–10	–	+10	µA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = –200 µA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
TIMING (note 5)					
F6 (Fig.3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
CLKO, F1/F6, R, G, B, $\overline{\text{VDS}}$					
$\overline{\text{FS}}$/$\overline{\text{DDA}}$, $\overline{\text{OD}}$ (notes 6, 7 and Fig.6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{\text{VDS}}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ floating after $\overline{\text{OD}}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{\text{VDS}}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{\text{VDS}}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ active after $\overline{\text{OD}}$ rise	t_{UOD}	0	–	60	ns
CLKO HIGH to $\overline{\text{FS}}$/$\overline{\text{DDA}}$ change	t_{DCH}	10	–	60	ns
$\overline{\text{FS}}$/$\overline{\text{DDA}}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 8)	t_{F1H}	–	500	–	ns
F1 LOW time (note 8)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{\text{OD}}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{\text{OD}}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 9, 10 and Fig.7)					
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{\text{UDS}}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{\text{AS}}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{\text{AS}}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{\text{UDS}}$ fall	t_{AFS}	0	–	–	ns
$\overline{\text{AS}}$ LOW to $\overline{\text{UDS}}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{\text{AS}}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{\text{AS}}$ LOW time	t_{LAS}	320	–	–	ns

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	275	ns
Link-through buffers					
(notes 9, 10 and Fig.8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from FTFROM					
(Fig.9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Microprocessor WRITE to FTFROM (Fig.10)					
Write cycle time (note 11)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig.11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig.12 for timing relationships and Fig.13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally.
2. Value under investigation
3. 16-level analogue voltage outputs.
4. Output voltage guaranteed when programmed for top level.
5. All timings are related to a 6,00 MHz clock.
6. CLKO, R, G, B, F1/F6, $\overline{VDS}$: C_L = 25 pF.
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
7. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
8. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
9. C_L = 150 pF.
10. Reference levels = 0,8 to 2,0 V.
11. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.

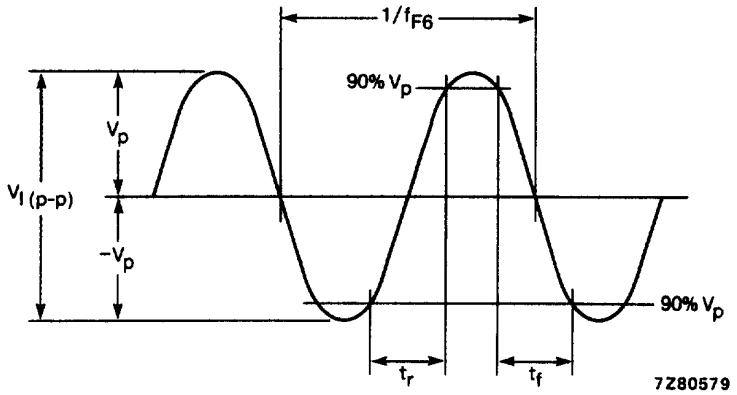
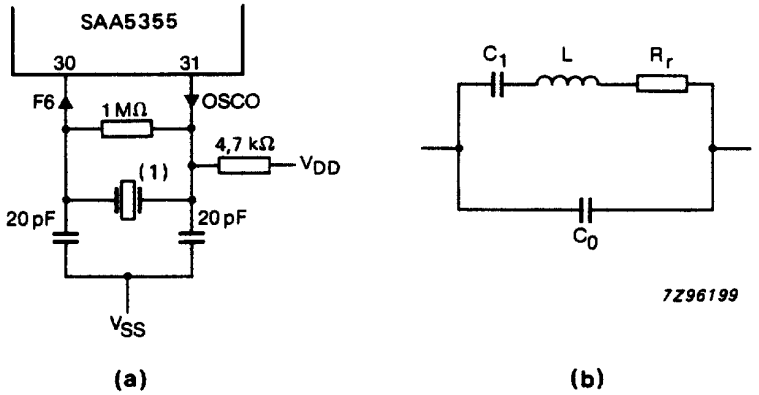


Fig.3 F6 input waveform.



(1) for 525-line operation, frequency = 6,041957 MHz.

Fig.4 (a) Oscillator circuit for SAA5355 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

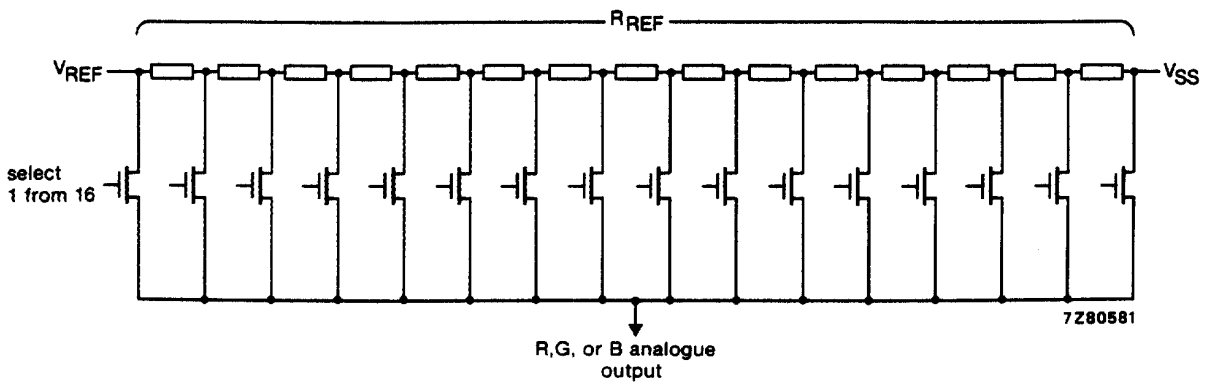


Fig.5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

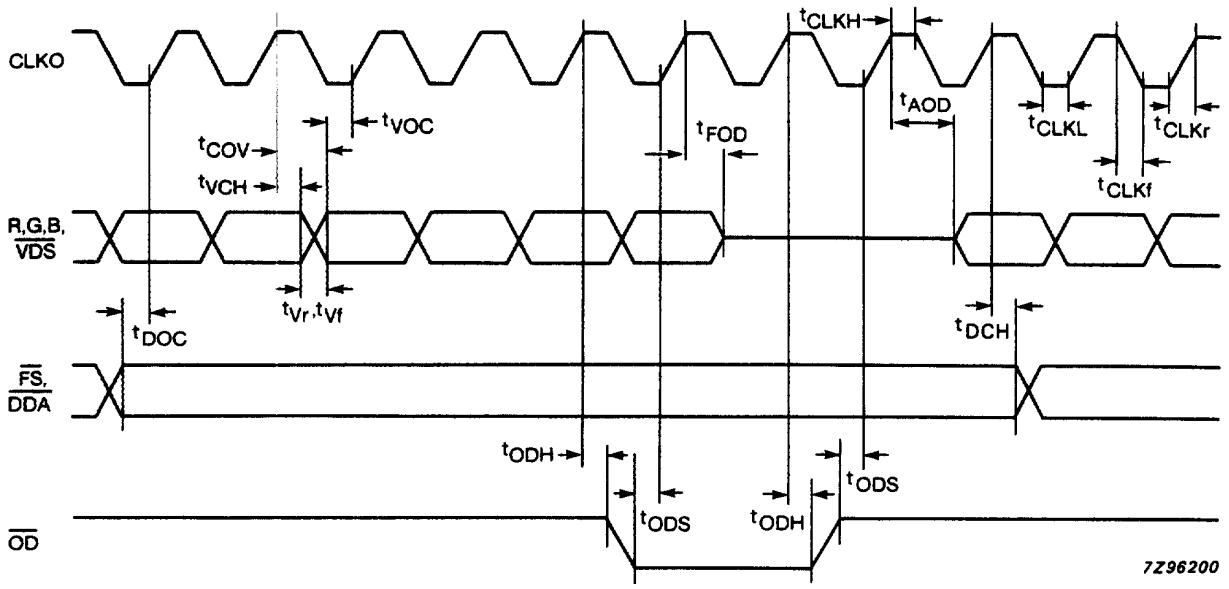


Fig.6 Video timing.

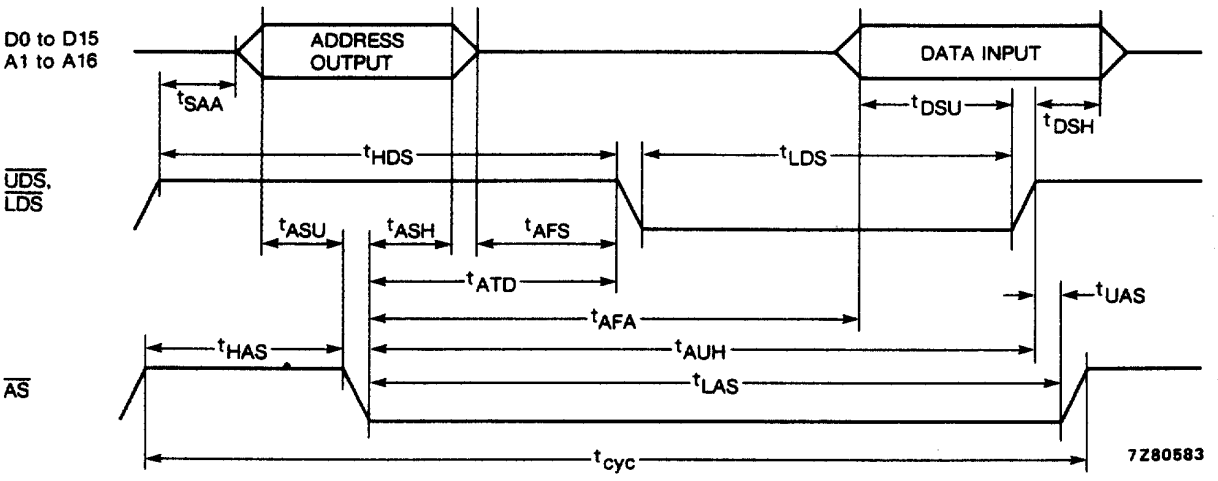


Fig.7 Memory access timing.

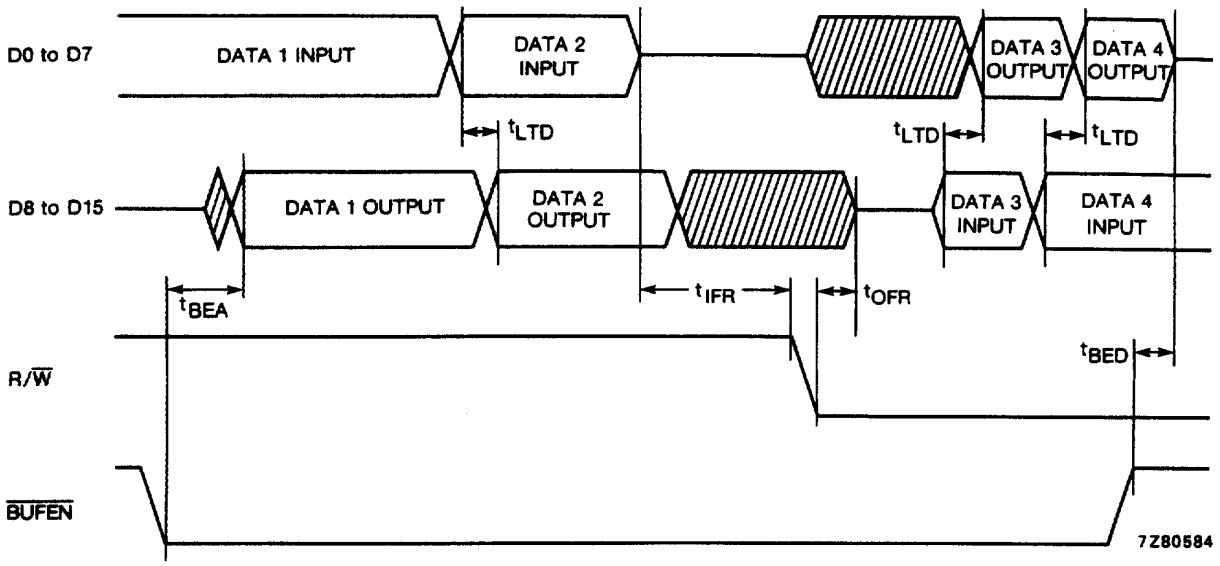


Fig.8 Timing of link-through buffers.

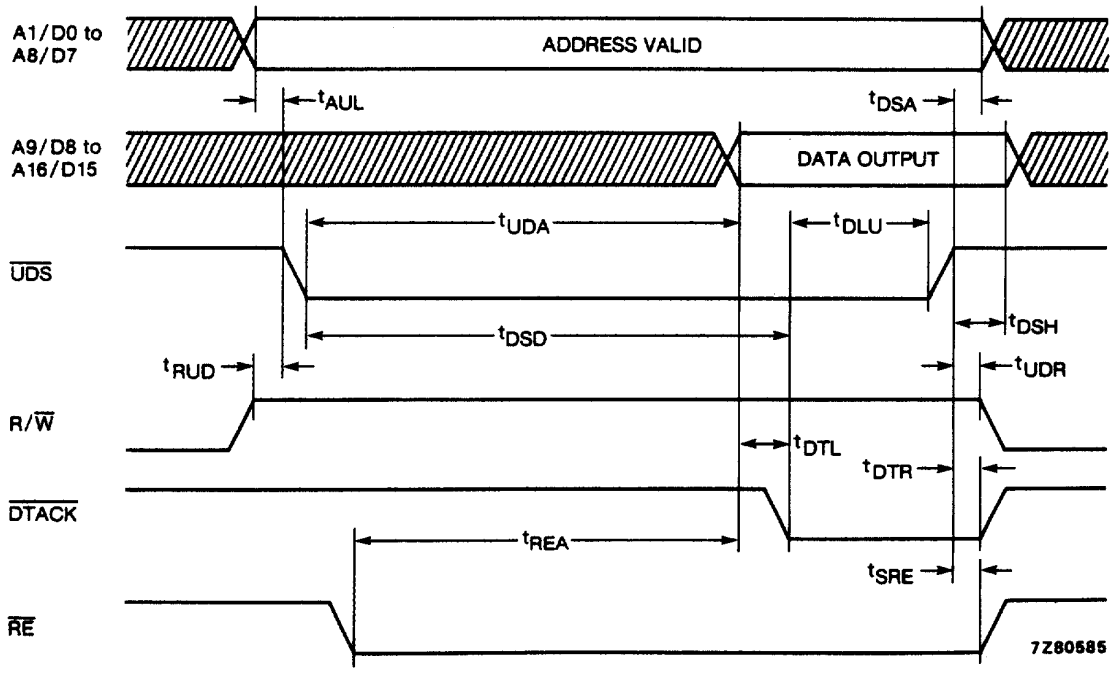


Fig.9 Timing of microprocessor read from FTFROM.

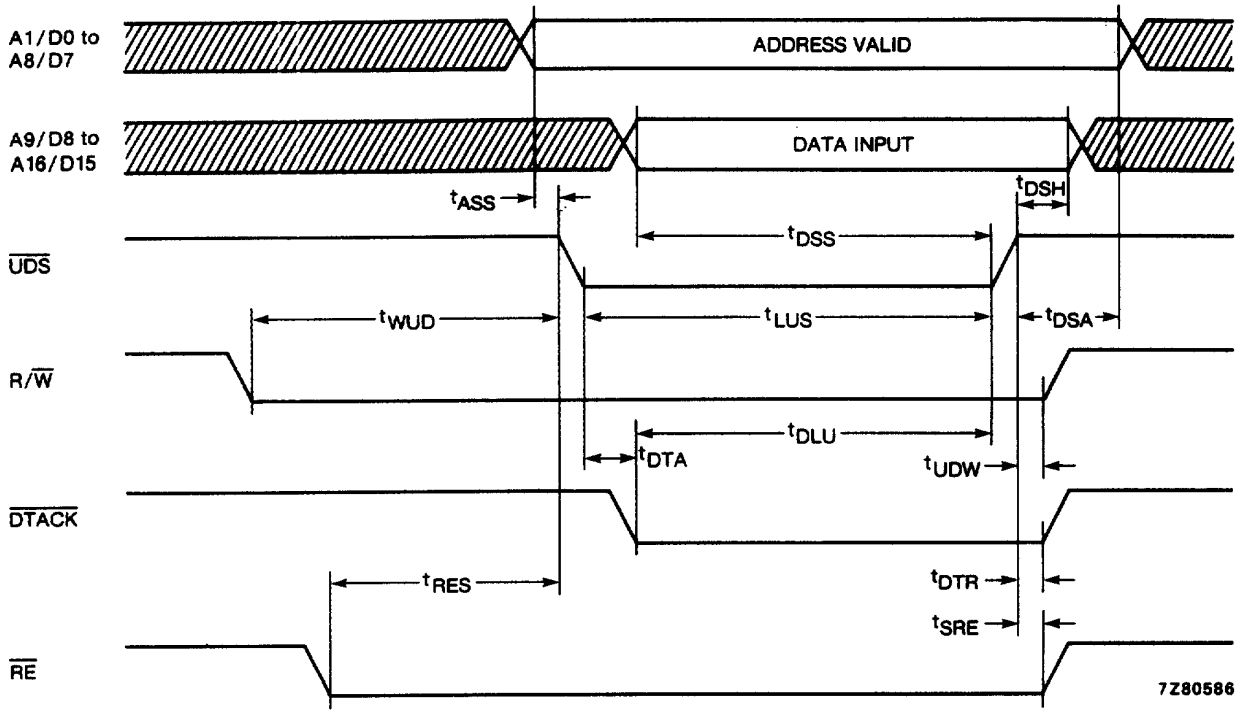


Fig.10 Timing of microprocessor write to FTFROM.

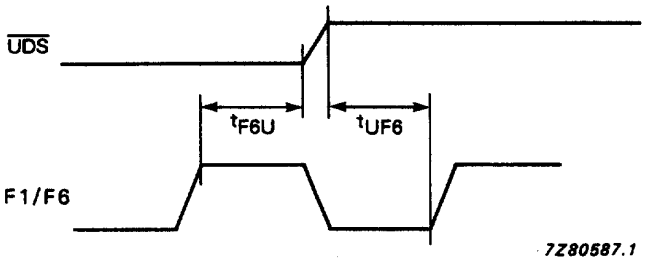


Fig.11 Timing of F1/F6 to memory access cycle.

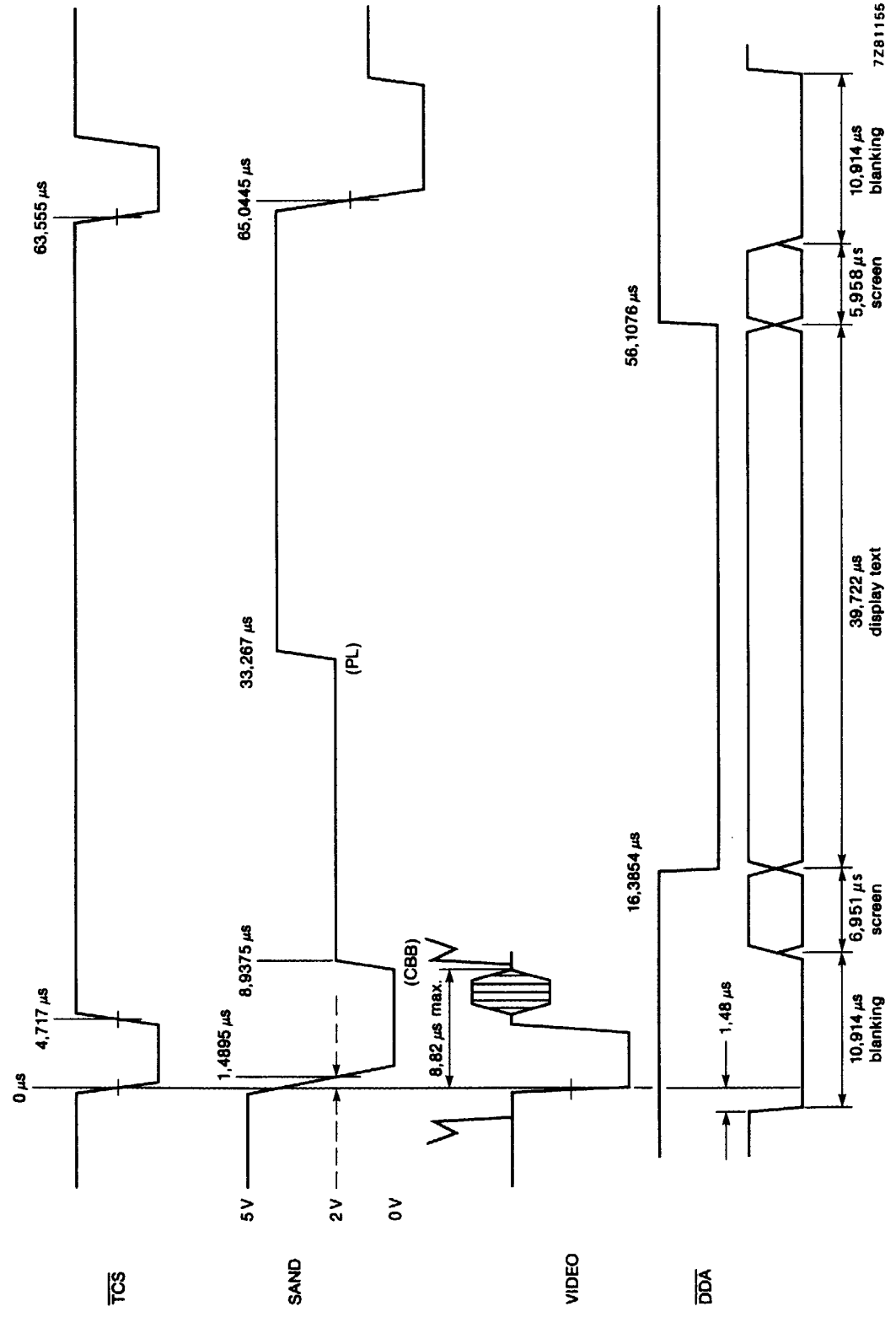


Fig.12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 6,041957 MHz.

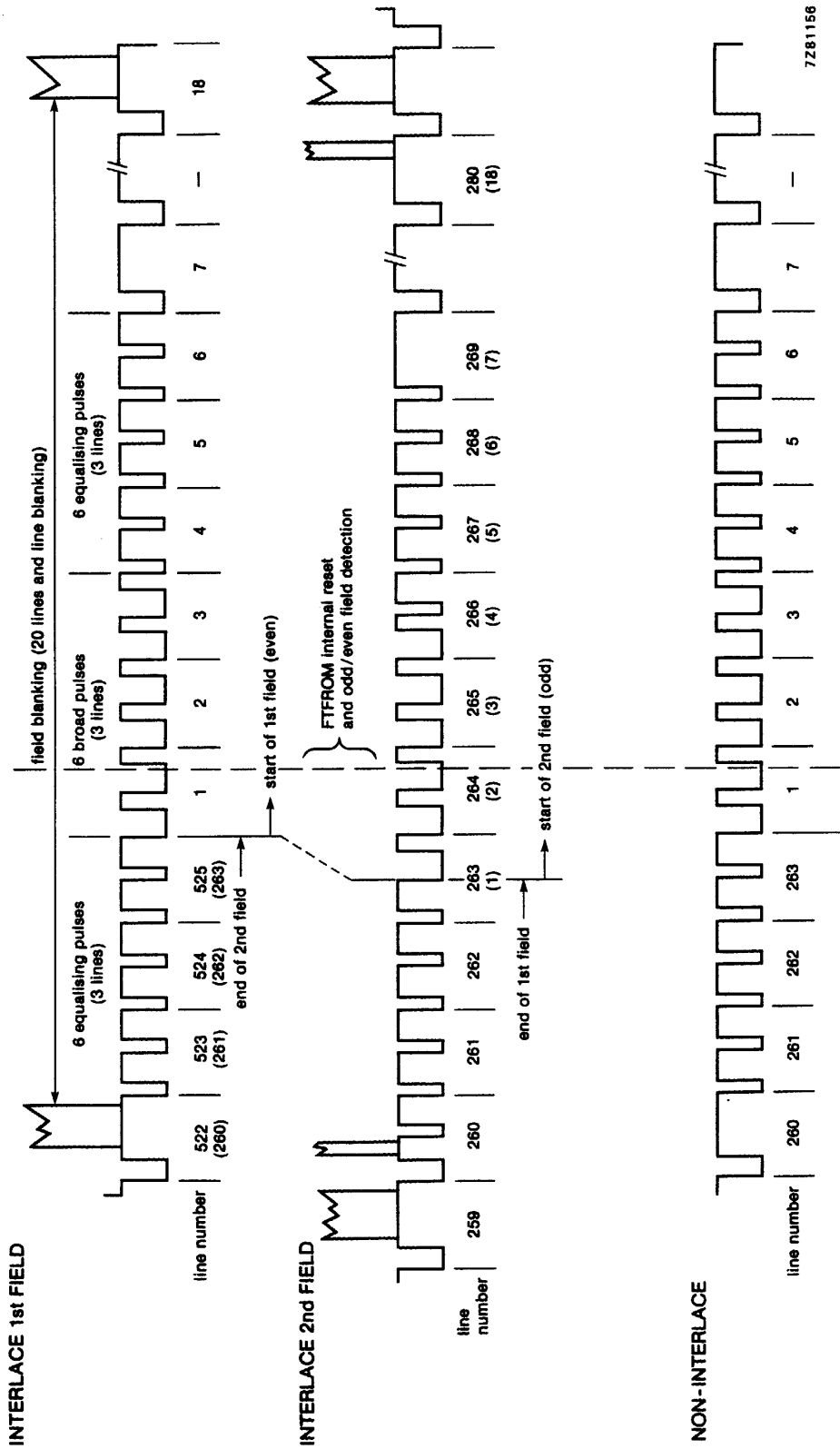


Fig.13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,717 µs; equalizing pulse widths = 2,23 µs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig.14, reference should also be made to the block diagram Fig.1.

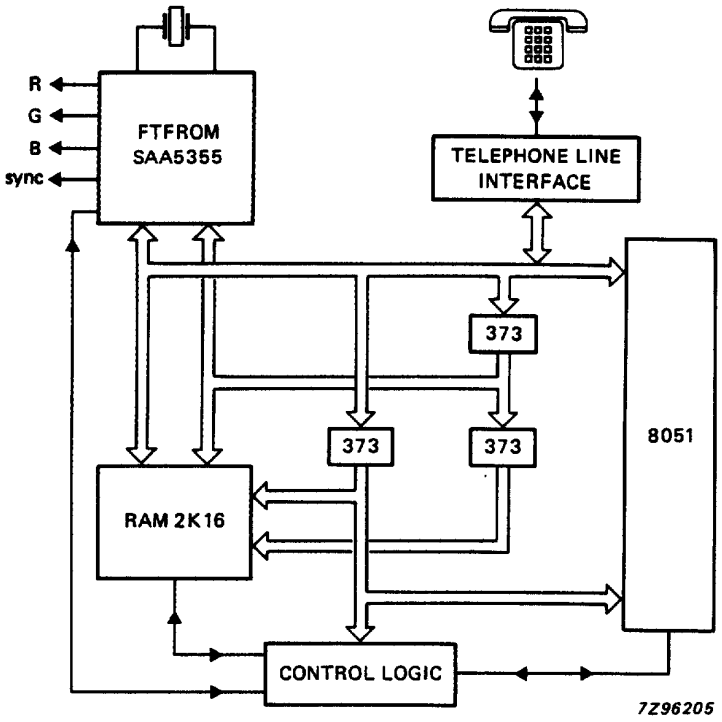


Fig.14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows — each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6,041957 MHz clock or an on-chip fixed-frequency crystal oscillator.
The basic video format is 40 characters per row, 20/21 rows per page and 10 video lines per row. FTFROM will also operate with 25 rows per page and 9 video lines per row.
The display is generated to the normal 525-line/59,94 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at approximately 1 MHz or 6 MHz (pin 29) is available for driving other devices, and a clock output (pin 27) is available for hard-copy dot synchronization.
A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

Character generation

FTFROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The fixed character tables (Tables 0 to 3), shown in Figs 15 and 16, are applicable to 10-lines-per-row applications. For 9 lines per row applications, the characters will be as shown but with the last line removed from alpha characters and line 5 (labelling 0 to 9) removed from mosaic and line drawing characters.

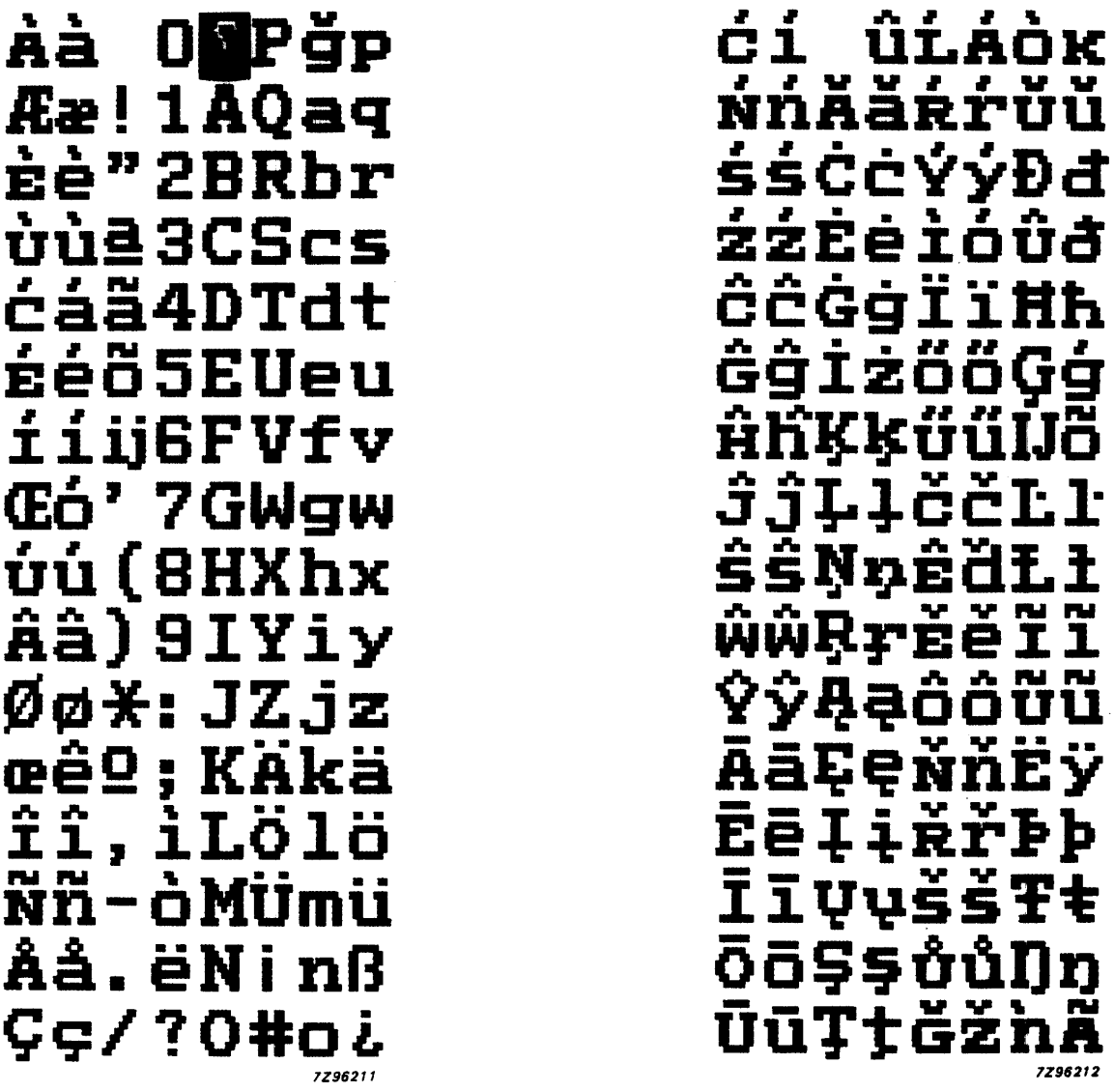
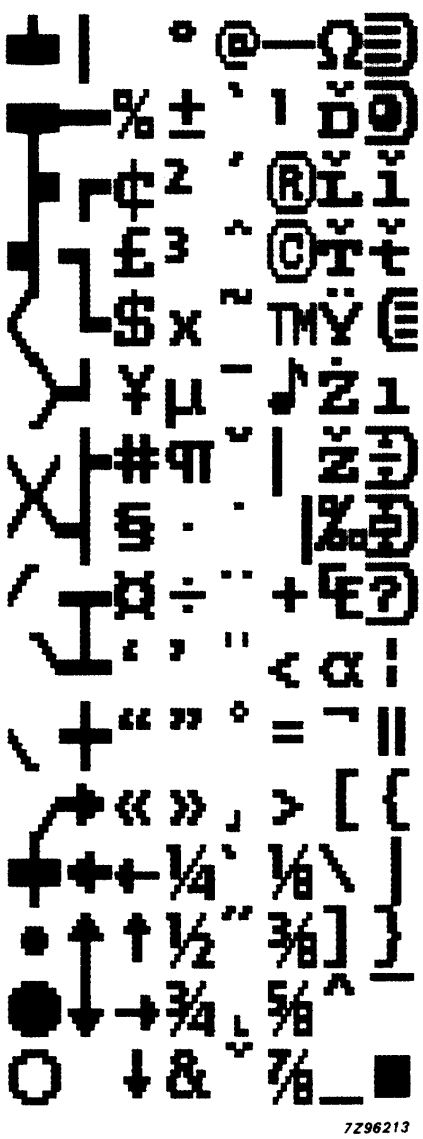
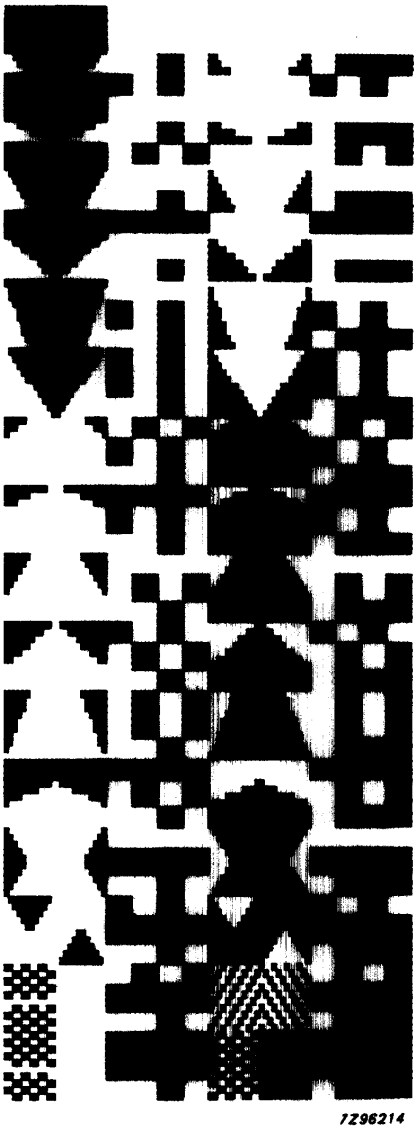


Fig.15 On-chip characters: (a) Table 0; (b) Table 1.



(a)



(b)

Fig.16 On-chip characters: (a) Table 2; (b) Table 3.

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2.
Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a ‘bit map’. All ROM-based characters and all display attributes remain available.

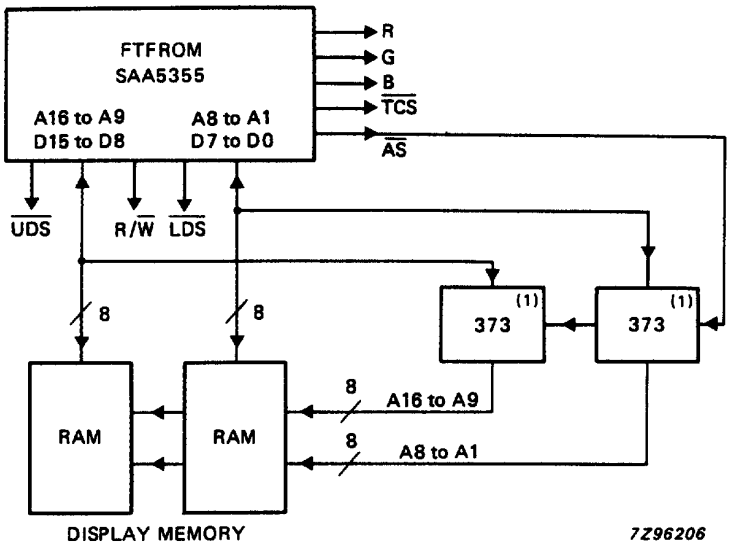
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- FTFROM fetches data from the display memory
- The microprocessor reads from, or writes to, FTFROM’s internal register map
- The microprocessor accesses the display memory

FTFROM access to display memory (Figs 17 and 18)

FTFROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 496,5 ns (F6 = 6,041957 MHz). The address strobe ($\overline{AS}$) signal from FTFROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/W is included although FTFROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig.17 Simply RAM interface circuit for display memory access.

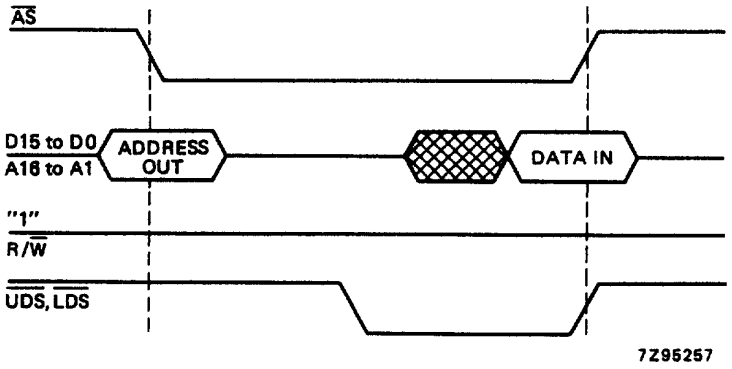


Fig.18 Bus timing for display memory access.

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig.19. The word addresses are numerically the same as the upper byte that they contain - there are no odd-numbered word addresses.

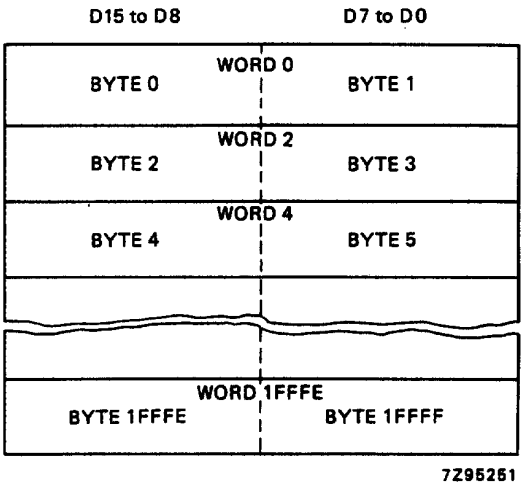


Fig.19 Display memory word/byte organization.

Warning time

As FTFROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by FTFROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and FTFROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that FTFROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of FTFROM's bus activity is programmable to be between 0 and 22,84 μs.

Microprocessor access to register map

FTFROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig.20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

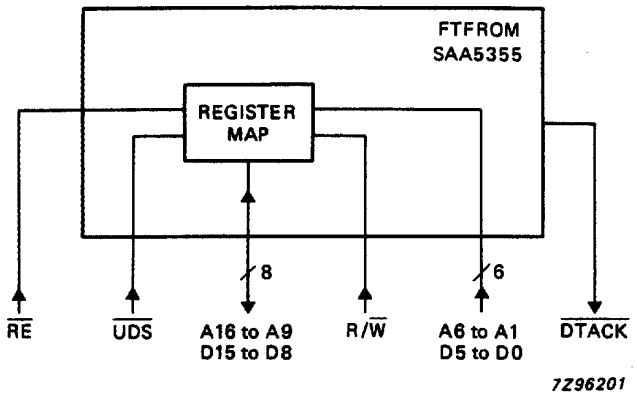


Fig.20 Microprocessor access to register map.

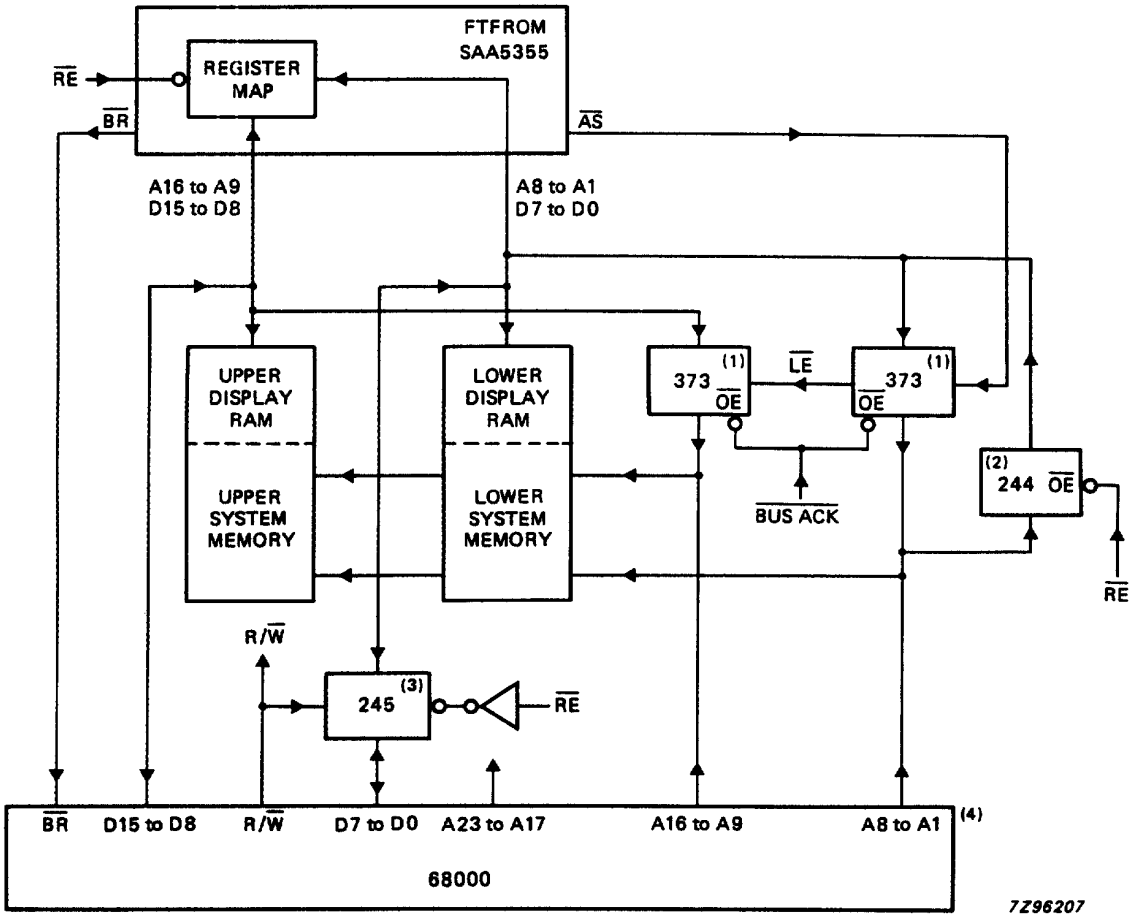
The main data and address paths used in a connected 68000 interface are shown in Fig.21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to FTFROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by FTFROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of FTFROM's scroll map contents at a location in its main memory.

8-bit microprocessors

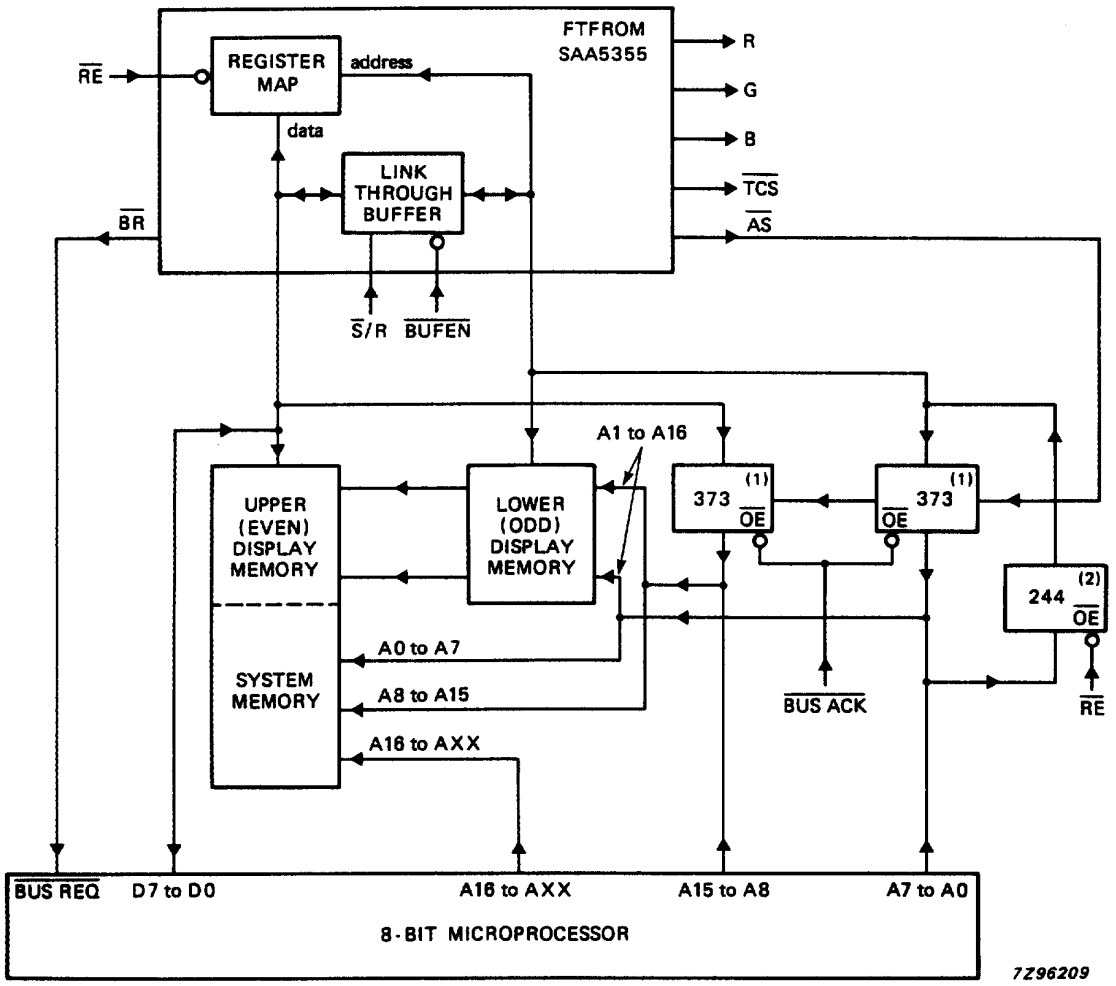
Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, FTFROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by FTFROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig.22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal transceiver (3-state)
(4) SCN6800 microprocessor unit

Fig.21 Connected 16-bit microprocessor system.

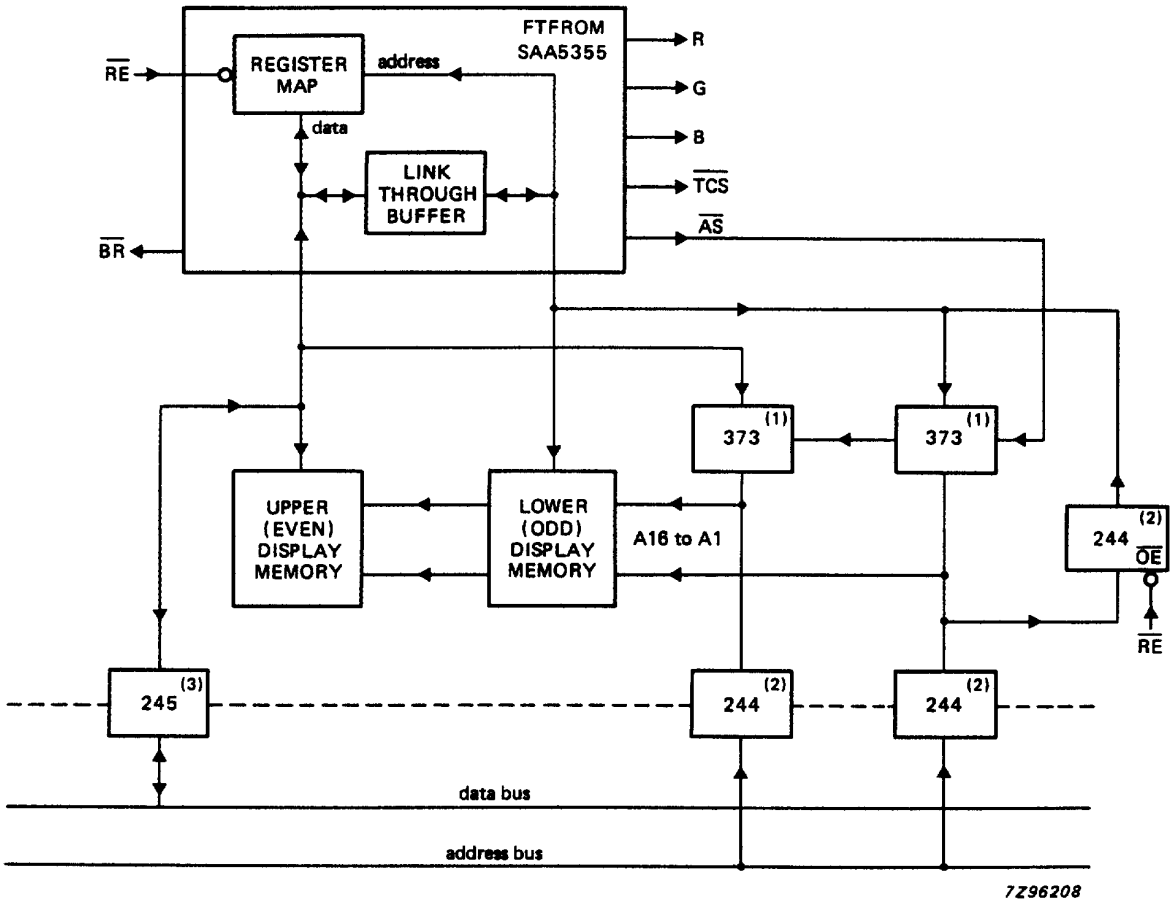


(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig.22 Connected 8-bit microprocessor system.

Disconnected systems

For many applications it may be desirable to disconnect FTFROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig.23. The two parts of the system then operate independently and communicate only when the microprocessor accesses FTFROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)

Fig.23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) FTFROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6,041957 MHz on-chip oscillator using an external crystal as shown in Fig.24.

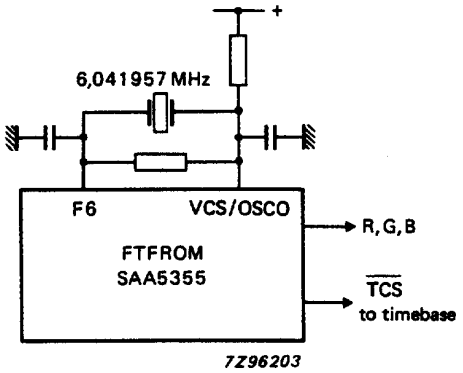


Fig.24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode FTFROM synchronizes directly to another device as shown in Fig.25. FTFROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using FTFROM's internal field sync separator.

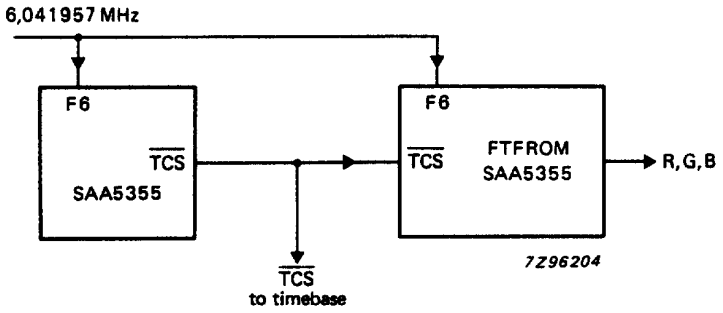


Fig.25 Simple-slave (direct sync) mode.

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig.26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When FTFROM is active, its horizontal counter forms part of the phase control loop — a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to FTFROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from FTFROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

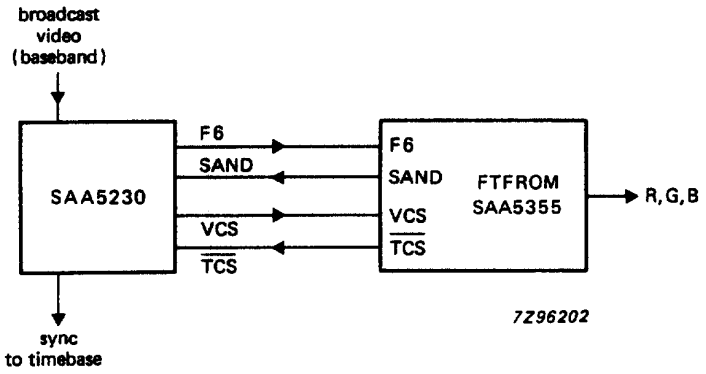
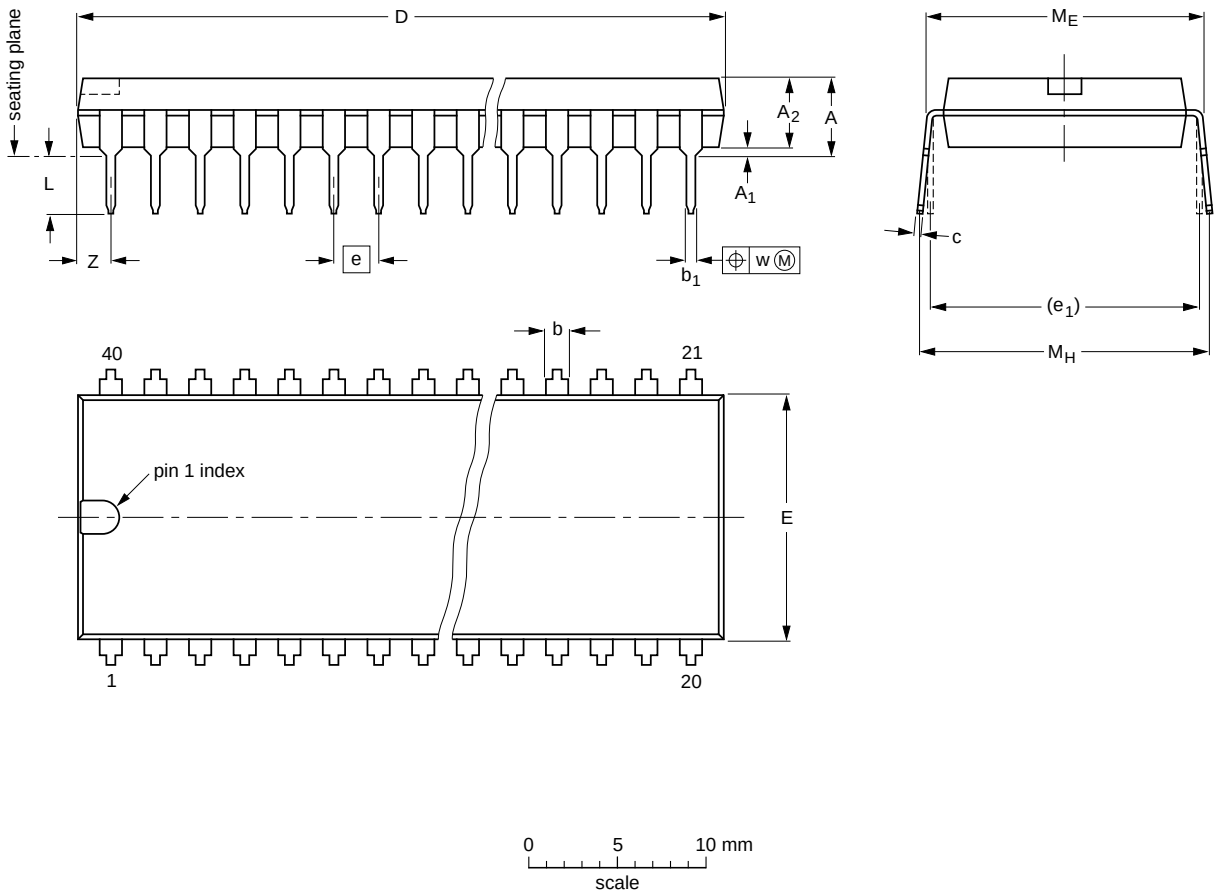


Fig.26 Phase-locked slave (indirect sync) mode.

PACKAGE OUTLINE

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.