DATA SHEET

SAA2002
Stereo filter and codec

Product specification
December 1993
Supersedes data of February 1993
File under Integrated Circuits, Miscellaneous

Philips Semiconductors

PHILIPS

Stereo filter and codec SAA2002

FEATURES

- Stereo filtering and codec functions in a single chip
- Drive processing interface
- Filtered data interface
- Baseband audio data interface
- LT interface to microcontroller
- Clock generator
- Low operating voltage capability.

GENERAL DESCRIPTION

The SAA2002 performs the sub-band filtering and audio frame codec functions in a Precision Adaptive Sub-band Coding (PASC) system. It is capable of functioning as a stand-alone decoder, but requires the addition of an Adaptive Allocation and Scale factor processor (SAA2012) in order to perform PASC encoding in a DCC record system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2002GP	44	QFP (1)	plastic	SOT205AG

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the Quality Reference Pocketbook are followed. The pocketbook can be ordered using the code 9398 510 34011.

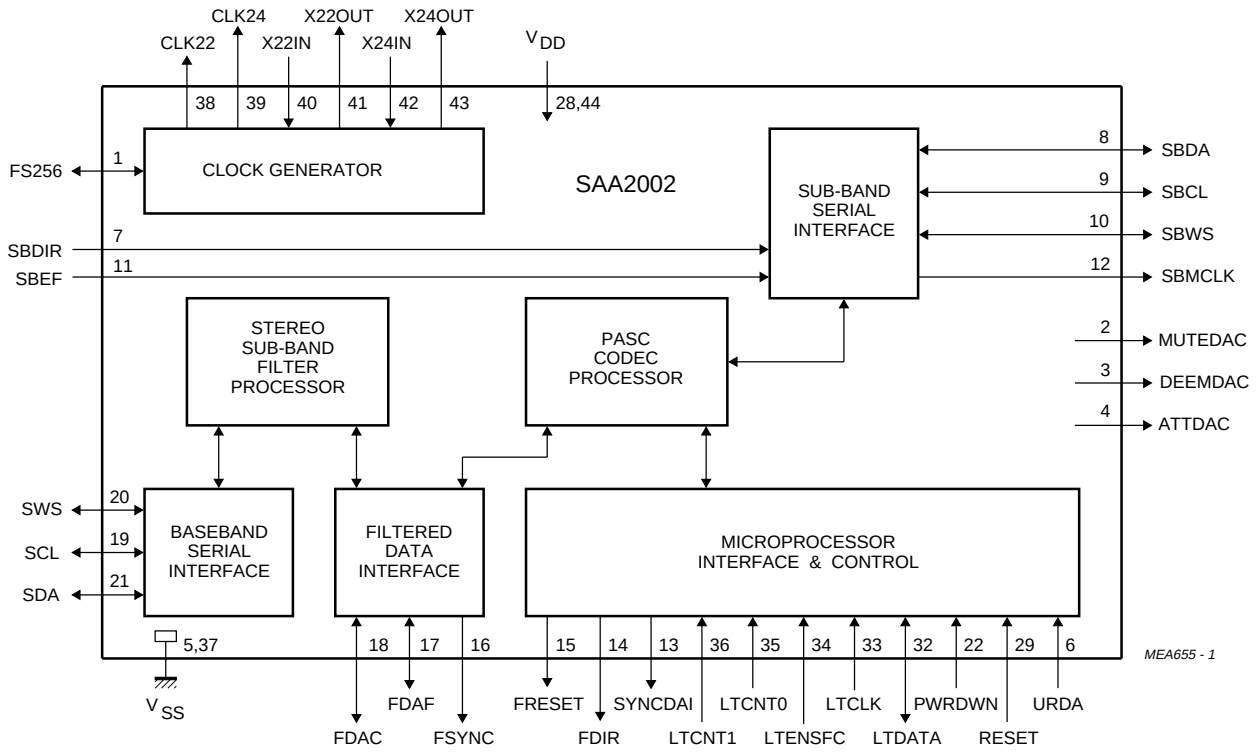


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FS256	1	filtered-I²S clock; 256 x f_s; 12 mA, 3-state output + CMOS input with pull-down
MUTEDAC	2	DAC control/output expander
DEEMDAC	3	DAC control/output expander
ATTDAC	4	DAC control/output expander
V_{SS}	5	supply ground (0 V)
URDA	6	unreliable drive processing data; CMOS level
SBDIR	7	sub-band I²S direction: (SWBS, SBCL, SBDA); CMOS level
SBDA	8	sub-band I²S data; 4 mA, 3-state output + CMOS input with pull-down
SBCL	9	sub-band I²S bit-clock; 4 mA, 3-state output + CMOS input with pull-down
SBWS	10	sub-band I²S word select; 4 mA, 3-state output + CMOS input with pull-down
SBEF	11	sub-band I²S byte error flag input; CMOS level
SBMCLK	12	sub-band I²S clock; 6.144 MHz locked to FS256; 8 mA, 3-state output + CMOS input with pull-down
SYNCDAI	13	Digital Audio Interface (DAI) synchronization pulse
FDIR	14	filtered-I²S direction: (FDAC, FDAF and SDA)
FRESET	15	reset signal for SAA2012
FSYNC	16	filtered-I²S synchronization signal for SAA2012
FDAF	17	filtered-I²S sub-band filter data; 4 mA, 3-state output + CMOS input with pull-down
FDAC	18	filtered-I²S sub-band codec data; 4 mA, 3-state output + CMOS input with pull-down
SCL	19	I²S bit-clock; 4 mA, 3-state output + CMOS input with pull-down
SWS	20	I²S word select; 4 mA, 3-state output + CMOS input with pull-down
SDA	21	I²S baseband data filter; 4 mA, 3-state output + CMOS input with pull-down
PWRDWN	22	sleep mode; CMOS level
DSC4	23	test pin; not to be connected
DSC3	24	test pin; not to be connected
DSC2	25	test pin; not to be connected
DSC1	26	test pin; not to be connected
DSC0	27	test pin; not to be connected
V_{DD}	28	supply voltage (+5 V)
RESET	29	system reset input; CMOS level with pull-down and hysteresis
T1	30	test pin; not to be connected
T0	31	test pin; not to be connected
LTDATA	32	LT interface data; 4 mA, 3-state output + CMOS input with pull-down
LTCLK	33	LT interface bit clock input; CMOS level
LTENSFC	34	LT interface enable input; CMOS level
LTCNT0	35	LT interface control input; CMOS level
LTCNT1	36	LT interface control input; CMOS level
V_{SS}	37	supply ground (0 V)
CLK22	38	22.5792 MHz buffered output
CLK24	39	24.576 MHz buffered output

SYMBOL	PIN	DESCRIPTION
X22IN	40	22.5792 MHz crystal input
X22OUT	41	22.5792 MHz crystal output
X24IN	42	24.576 MHz crystal input
X24OUT	43	24.576 MHz crystal output
V_{DD}	44	supply voltage (+5 V)

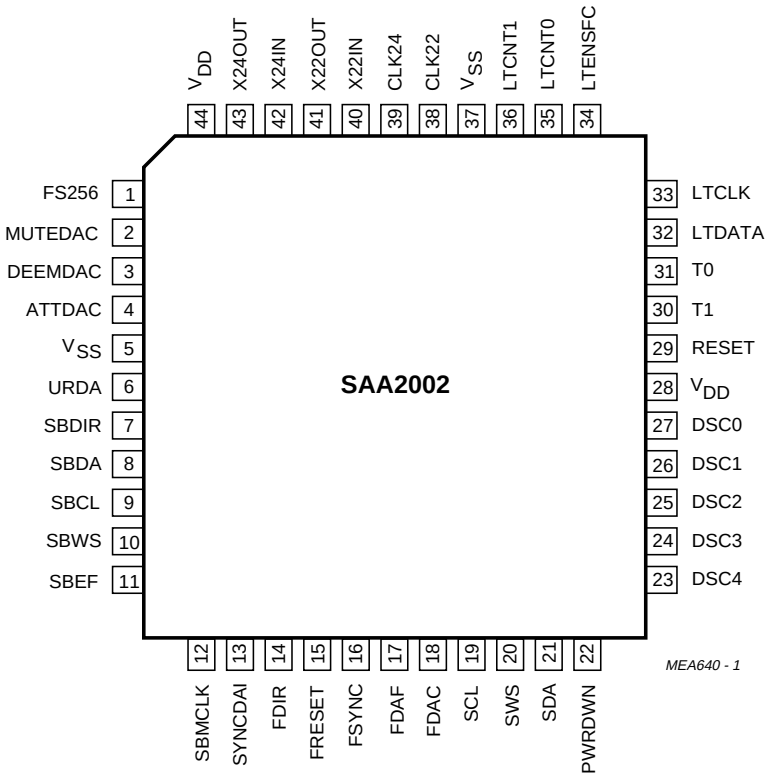


Fig.2 Pin configuration.

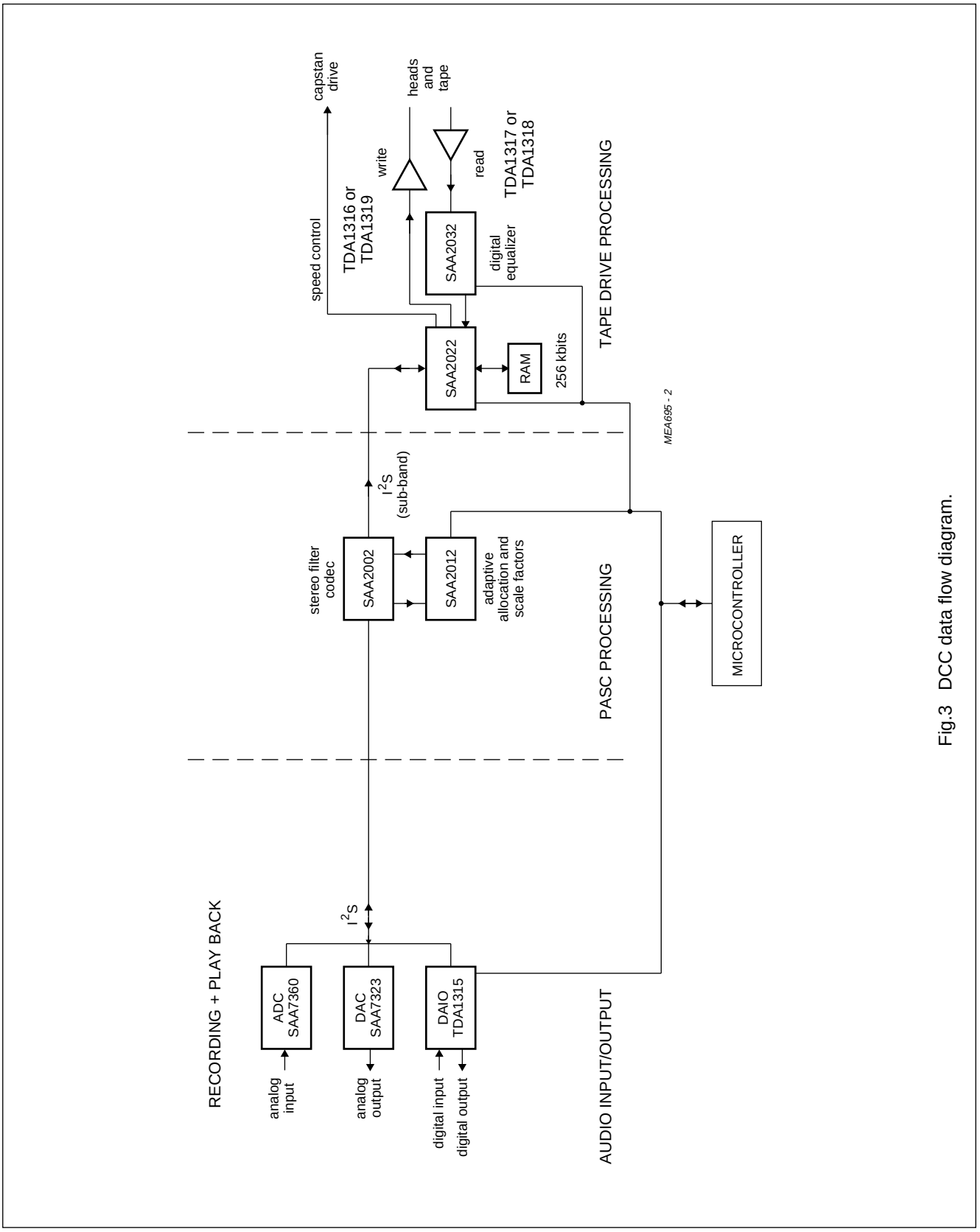


Fig.3 DCC data flow diagram.

FUNCTIONAL DESCRIPTION

PASC

Precision Adaptive Sub-band Coding achieves highly efficient digital encoding of audio signals by using an algorithm based on the characteristics of the human auditory system.

The broad-band audio signal is split into 32 sub-band signals during encoding. For each of the sub-band signals the masking threshold is calculated. The samples of the sub-bands are incorporated in the PASC signal with an accuracy that is determined by the signal to masking threshold ratio for that sub-band.

During decoding, the sub-band signals are reconstructed and combined into a broadband audio signal. The integrated filter processor performs the splitting (encoding) and joining (decoding) including the corresponding formatting functions.

For encoding, a SAA2012 is necessary to calculate the masking threshold and required accuracy of the sub-band samples.

Encoding (see Fig.4)

An encoding algorithm table is used during the recording process but, due to the Adaptive Allocation functions of the SAA2012, this may change with every frame. The table is therefore calculated for each frame by the SAA2012 and then transferred to the SAA2002.

A frame contains 2 x 384 samples of Left and Right audio data. This results in 12 samples per sub-band (32 sub-bands). The samples of the greatest amplitude are used to determine the scale factor for a given sub-band. All samples are then scaled to represent a fraction of the greatest amplitude.

Once scaled, the samples are quantified to reduce the number of bits to correspond with the allocation table as calculated by the SAA2012. Synchronization and coding information data is then added to result in a fully encoded PASC signal.

Decoding (see Fig.5)

All essential information (synchronization, system information, scale factors and encoded sub-band samples) are conveyed by incoming data. Decoding is repeated for every frame.

After sync and coding information, allocation data and the scale factors are used to correctly fill the scale factor array. This is followed by a process of multiplication to provide de-quantification and de-scaling of the PASC samples. The decoded sub-band samples, which are represented in 24-bit two's complement notation, are processed by the sub-band filters and reconstituted into a single digital audio signal.

RESET

Reset must be active from system power-up, or the end of sleep mode (falling edge of PWRDWN), for a period equivalent to 24 cycles of CLK24 plus the crystal oscillator start-up time.

Sleep mode

A HIGH input applied to the PWRDWN pin will halt all internally generated clock signals. As a result, chip activity will halt completely with outputs frozen in the state which was current at the time of PWRDWN activation. The bi-directional outputs: LTDATA, FDAC, FDAF, SDA, SBWS, SBCL and SBDA will be in 3-state.

Crystal Oscillators

A 24.576 MHz crystal together with some external components form the 24.576 MHz oscillator (pins 42 and 43). Similarly a 22.5792 MHz oscillator (pins 40 and 41) is performed by similar peripheral components together with an appropriate crystal (see Fig.6).

The component values shown apply only to crystals from the Philips 4322 156 series which exhibit an equivalent series resistance of $\leq 40\ \Omega$.

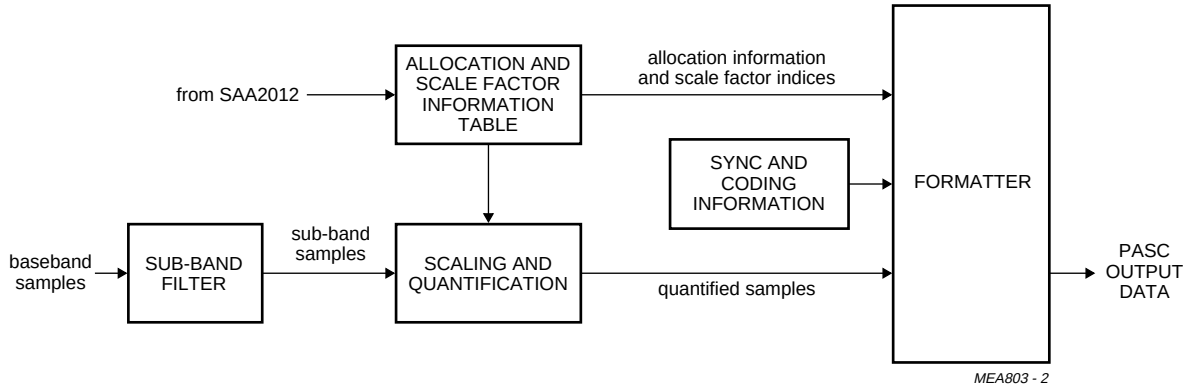


Fig.4 Encoding mode.

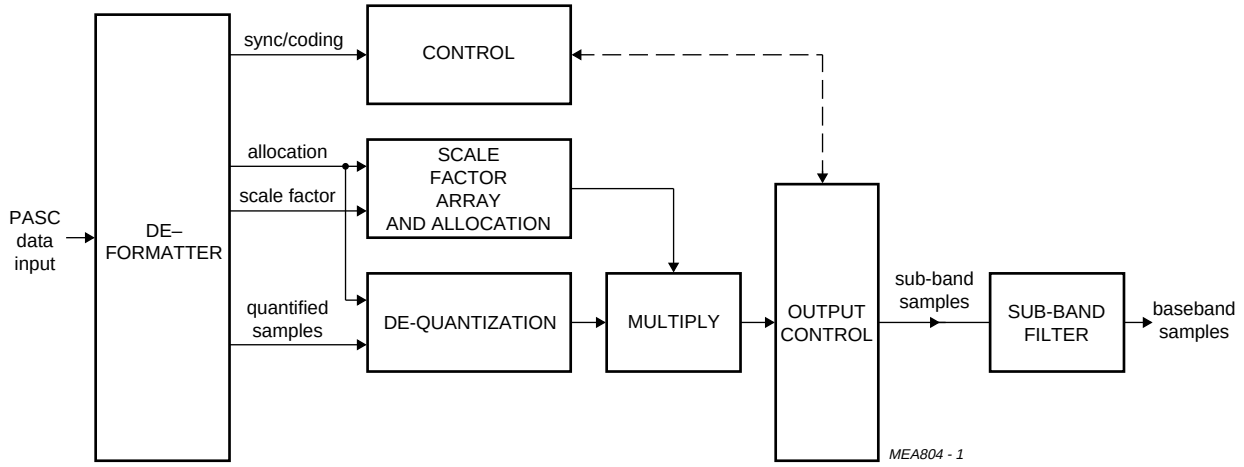
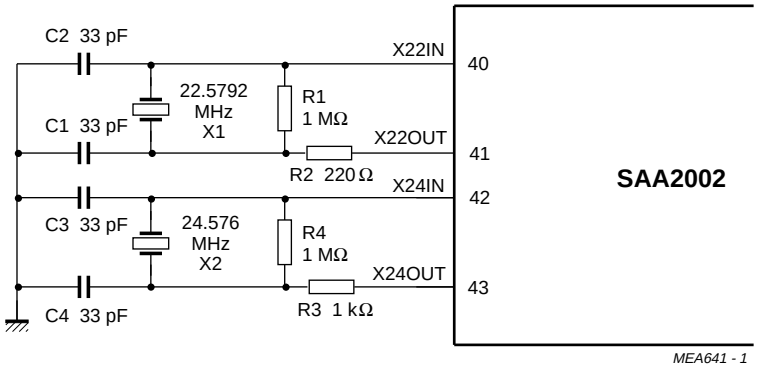


Fig.5 Decoding mode.



Component values apply only to crystals from the Philips 4322 156 series.

Fig.6 Crystal oscillator components.

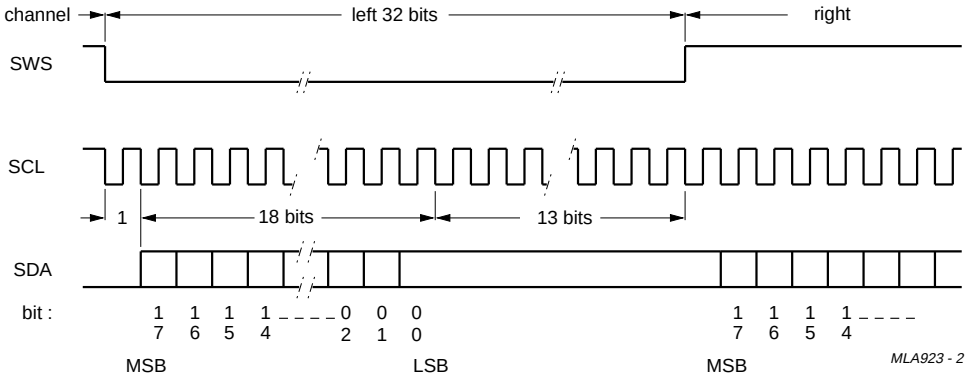


Fig.7 Transfer of SDA data (standard I^2S default format).

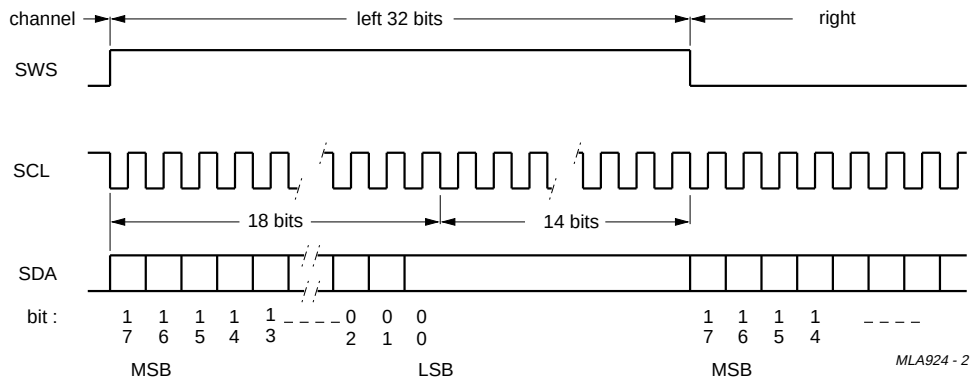


Fig.8 Transfer of SDA data (alternative format).

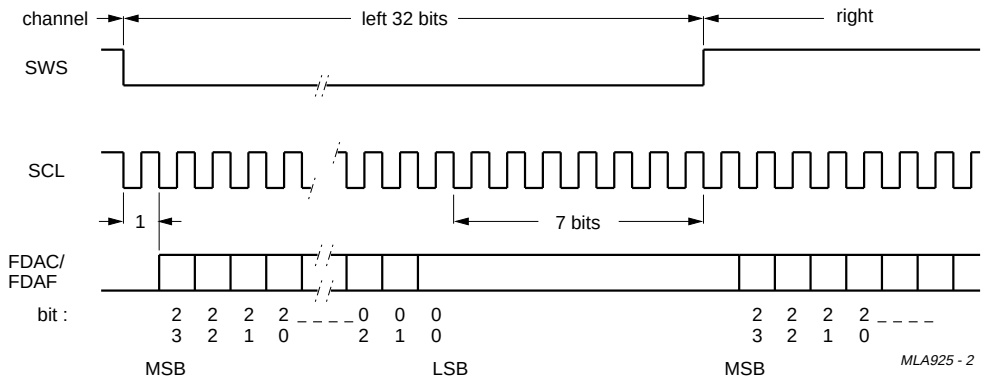


Fig.9 Transfer of FDAF and FDAC (filtered) data.

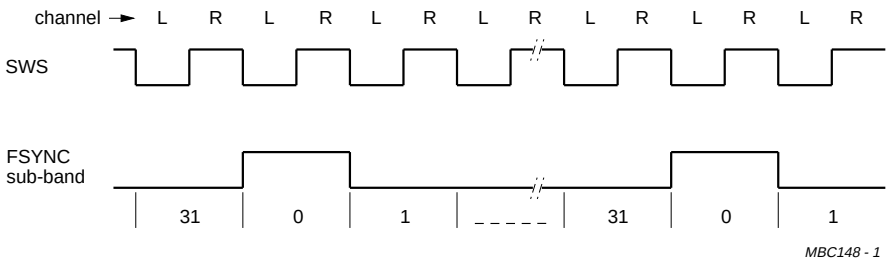


Fig.10 SWS related to phase of FSYNC.

Baseband Interface Signals

Table 1 Interface between the SAA2002 and the baseband input/output circuitry.

SIGNAL	MODE	DESCRIPTION	OPERATING FREQUENCY
SWS	bi-directional	word (channel) select	f_s
SCL	bi-directional	bit clock	$64f_s$
SDA	bi-directional	baseband data	–
FDIR	output	decoding mode (direction control)	–

The SWS signal indicates the channel of the sample signal (either Left or Right) and is equal to the sampling frequency f_s.

Operating at a frequency of 64 x f_s that is used for sampling, the bit clock dictates that each SWS period contains 64 SDA data bits. Of these, a maximum of 36 are used to transfer data (samples may have a length up to 18-bits). Samples are transferred most significant bit (MSB) first. Both SWS and SDA change state at the negative edge of SCL.

This baseband data is transferred between the SAA2002 and the input/output using either standard I^2S (default) or the alternative format shown in Fig.8.

Interface between SAA2002 and SAA2012

Table 2 Filtered I^2S interface.

SIGNAL	MODE	DESCRIPTION	OPERATING FREQUENCY
SWS	bi-directional	word select (common to I^2S)	f_s
SCL	bi-directional	bit clock (common to I^2S)	$64f_s$
FDAC	bi-directional	codec data	–
FDAF	bi-directional	filter data	–
FSYNC	output	synchronization	$f_s/32$

Filtered data is transferred between SAA2002 filter/codec functions and the SAA2012 using the format shown in Fig.9.

The frequency of the SWS signal is equal to the sample frequency f_s and the bit clock SCL is 64 times the sample frequency. Each period of SWS contains 64 data-bits, 48 of which are used to transfer data. The half period in which SWS is LOW is used to transfer the information of the Left channel while the following half period during which SWS is HIGH carries the data of the Right channel. The 24-bit samples are transferred Most Significant Bit (MSB) first. This bit is transferred in the bit clock period with a 1-bit delay following the change in SWS. Both SWS and FDAF/FDAC change state at the negative edge of SCL.

The SAA2012 may be synchronized to the sub-band codec using the FSYNC signal, which defines the SWS period in which the samples of sub-band 0 (containing the lowest frequency components) are transferred (see Fig.9).

SAA2012 AND INPUT/OUTPUT MODE CONTROL

The operation of SAA2012 and the input/output circuitry is controlled by three signals shown in Table 4.

FRESET and SYNCDAI are given whenever:

- FS256, SCL and SWS outputs switch between high and low impedance
- FS256 frequency is changed (12.288/11.2896/8.192 MHz)
- FDIR is switching
- The bit rate is changing
- System reset is active.

PASC CODED INTERFACE

The interface that carries the PASC coded signal uses the signals as indicated in Table 3.

Table 3 The PASC I^2S interface.

SIGNAL	MODE	DESCRIPTION
SBWS	bi-directional	word selection
SBCL	bi-directional	bit clock
SBDA	bi-directional	sub-band coded data
SBEF	input	error signal

Operation is further controlled by:

- SBDIR: input; direction of data flow
- URDA: input; unreliable encoded data signal.

The SBMCLK signal is the main frequency from which other clock signals are derived. In encode mode this division is performed internally. In decode mode the external source should provide SBWS and SBCL. The frequency of the signal is equal to 1/32nd of the bit rate. The frequency of the bit clock SBCL is twice that of the bit rate.

Table 4 SAA2012 input/output control.

SIGNAL	MODE	DESCRIPTION
FRESET	output	request a general reset of SAA2012
FDIR	output	logic 1 for decoding and logic 0 for encoding mode (common to I^2S)
SYNCDAI	output	pulse for synchronization of digital input/output (TDA1315)

ENCODE MODE

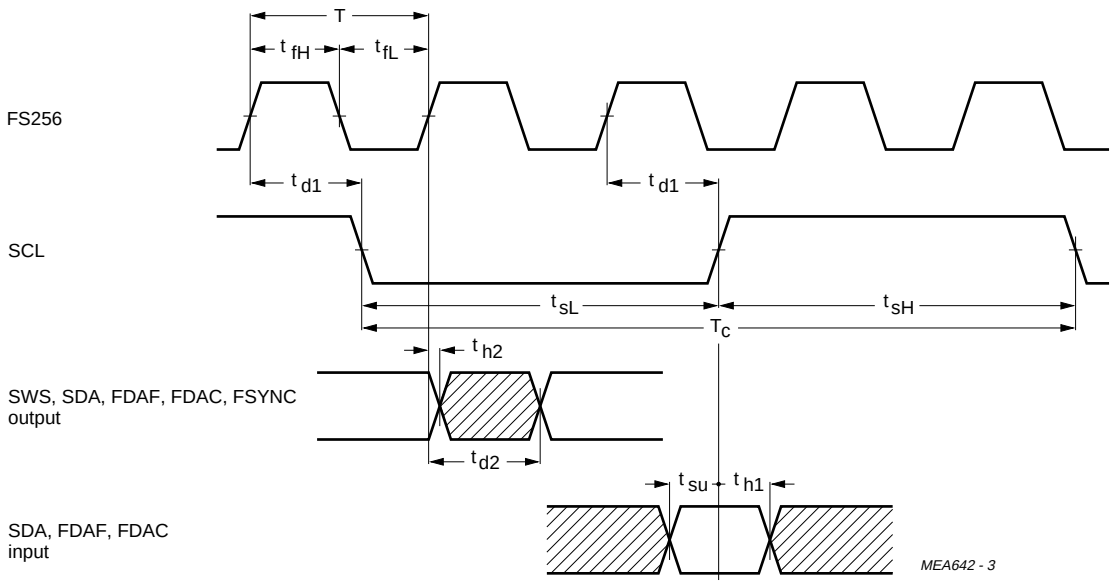
The following modes are supported:

Stereo or 2-channel mono at 384 kbits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.

DECODE MODE

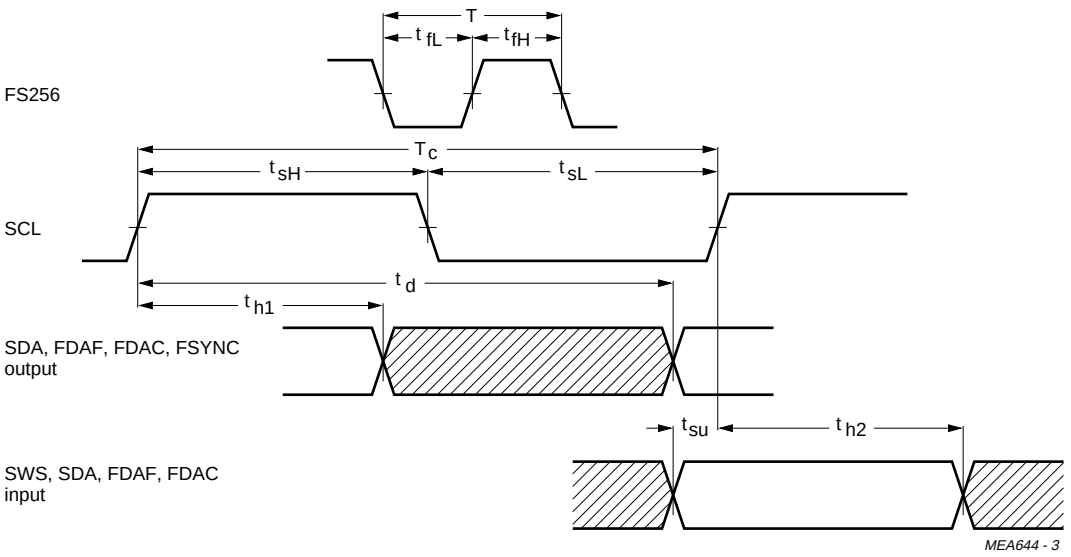
The following modes are supported:

Stereo and joint stereo, 2-channel mono and 1-channel mono at 384 kbits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.



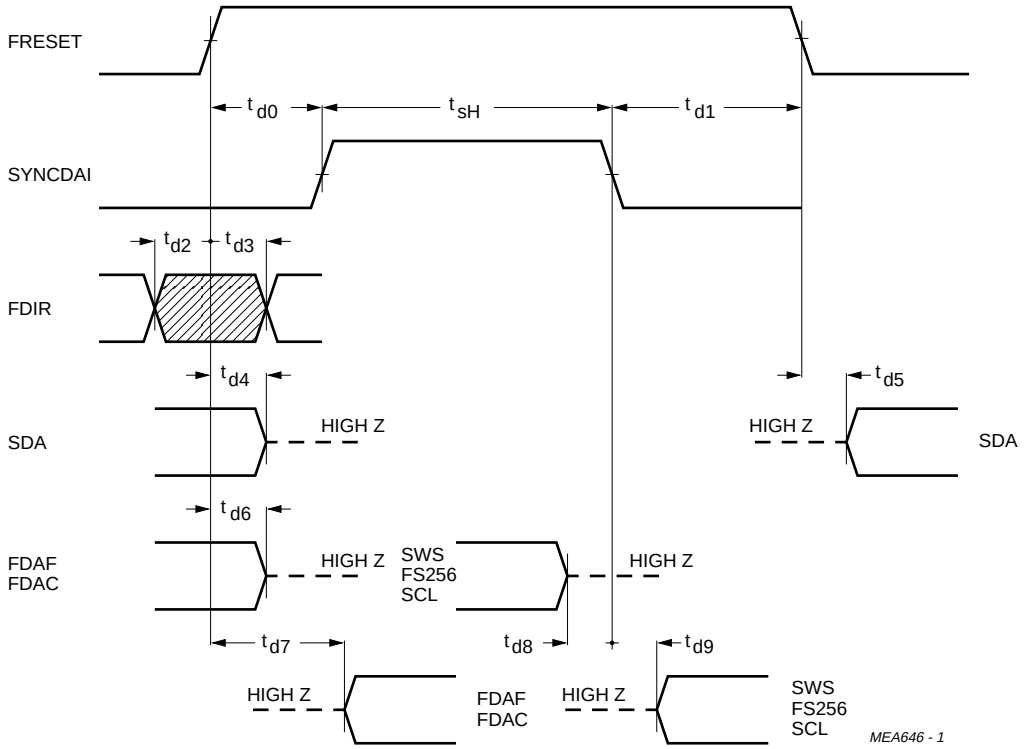
T	FS256 cycle time (f_s = 48 kHz)	81.4 ns nominal
	FS256 cycle time (f_s = 44.1 kHz)	88.6 ns nominal
	FS256 cycle time (f_s = 32 kHz)	122.1 ns nominal
T_c	SCL cycle time	4T ns nominal
t_{fH}	FS256 HIGH time (f_s = 48 kHz)	≥ 35 ns
	FS256 HIGH time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 HIGH time (f_s = 32 kHz)	≥ 75 ns
t_{fL}	FS256 LOW time (f_s = 48 kHz)	≥ 15 ns
	FS256 LOW time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 LOW time (f_s = 32 kHz)	≥ 75 ns
t_{sH}	SCL HIGH time	≥ 2T – 20 ns
t_{sL}	SCL LOW time	≥ 2T – 20 ns
t_{su}	SDA, FDAF and FDAC input set-up time before FS256 HIGH	≥ 20 ns
t_{h1}	SDA, FDAF and FDAC input hold time after FS256 HIGH	≥ 30 ns
t_{h2}	SDA, FDAF and FDAC output hold time after FS256 HIGH	≥ 0 ns
$t_{d1,2}$	FS256 HIGH to SCL, SWS, SDA, FDAF and FDAC output valid	≤ 50 ns

Fig.11 Filtered-I²S interface timing (master mode - FS256, SCL and SWS are output).



t_{fH}	FS256 HIGH time	≥ 35 ns
t_{fL}	FS256 LOW time	≥ 35 ns
t_{sH}	SCL HIGH time	≥ T + 35 ns
t_{sL}	SCL LOW time	≥ T + 35 ns
t_{su}	SDA, FDAF and FDAC input set-up time valid after SCL HIGH	≥ 20 ns
t_{h1}	SDA, FDAF and FDAC output hold time after SCL HIGH	≥ 2T – 15 ns
t_{h2}	SDA, FDAF and FDAC input hold time after SCL HIGH	≥ T + 20 ns
t_d	SCL HIGH to SDA, FDAF and FDAC output valid	≤ 3T + 60 ns

Fig.12 Filtered-I²S interface timing (slave mode - FS256, SCL and SWS are input).



t_{d0}	FRESET HIGH to SYNCDAI HIGH	≥ 300 ns
t_{sH}	SYNCDAI HIGH time	≥ 1280 ns
t_{d1}	SYNCDAI LOW to FRESET LOW	≥ 790 ns
t_{d2}	FDIR hold to FRESET HIGH	≤ 20 ns
t_{d3}	FRESET HIGH to FDIR valid	≤ 20 ns
t_{d4}	SDA change to high impedance after FRESET HIGH	≥ 0 ns and ≤ 170 ns
t_{d5}	SDA remains high impedance after FRESET LOW	≥ 0 ns and ≤ 170 ns
t_{d6}	FDAF and FDAC change to high impedance after FRESET HIGH	≤ 20 ns
t_{d7}	FDAF and FDAC remain high impedance after FRESET HIGH	≥ 460 ns
t_{d8}	FS256, SWS and SCL change to high impedance before SYNCDAI HIGH	≥ 140 ns
t_{d9}	FS256, SWS and SCL remain high impedance after SYNCDAI HIGH	≥ 140 ns

Fig.13 Mode switch timing.

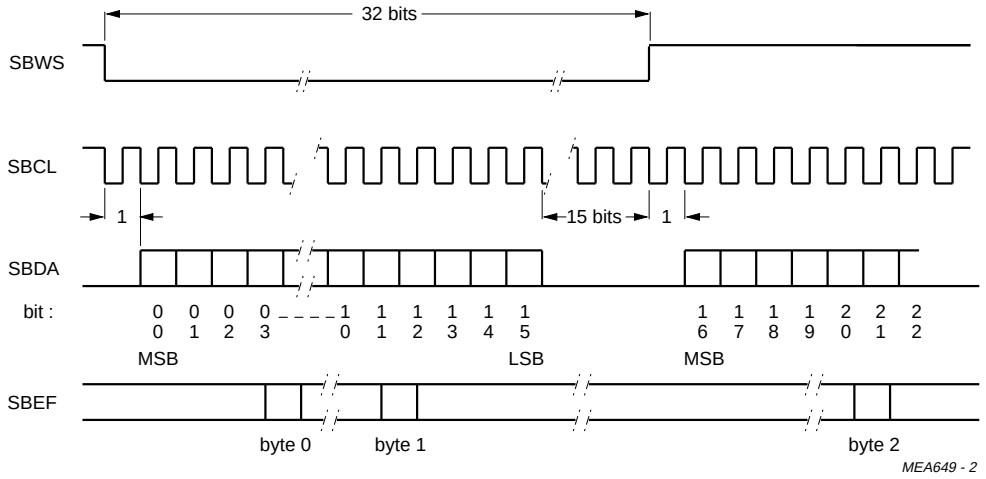


Fig.14 Transferring PASC data to and from the SAA2002.

PASC Coded Interface (sub-band I²S)

The PASC coded data is transferred to and from the SAA2002 using the format shown in Fig.15.

Each period of SBWS contains 64 data bits, 32 of which are used to convey data. The half-period during which SBWS is logic 0 is used to transfer the first 16-bits (0 to 15) of a sub-band slot. The remaining half-period during which SBWS is logic 1 carries the remaining 16-bits (16 to 31). Thus one period of SBWS corresponds with one slot of the sub-band signal.

Bits 0 and 16 are transferred in the bit clock period, one bit-time after the change in SBWS. Both SBWS and SBDA change state during the negative edge of SBCL.

In decode mode a byte error flag SBEF is also transferred. This occurs approximately in the middle of the corresponding byte (byte 0 = bits 0 to 7, byte 1 = bits 8 to 15 etc.).

ENCODING MODE

SBCL, SBWS and SBDA are generated by the SAA2002. However, if the SBDIR signal is logic 1, the output buffers are not enabled and these signals do not appear on the pins. This mode is available to permit a change of operating mode whilst the bus signals are driven from an external source.

DECODING MODE

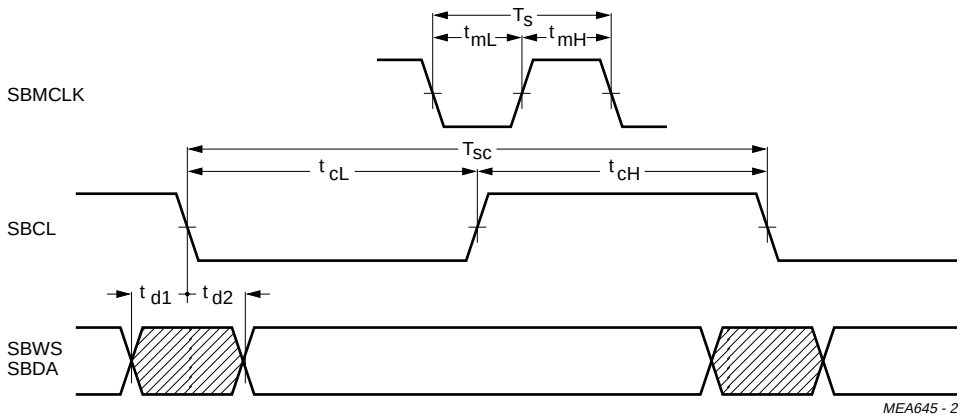
SBCL, SBWS and SBDA are generated by an external source.
Table 5 contains a summary of the source signals in the various modes.

Table 5 Modes and source signals.

MODE	FDIR	SBDIR	SOURCE					REMARKS
			SBWS	SBCL	SBDA	SBEF	SBMCLK	
Encode	0	0	INT	INT	INT	– – –	INT	note 1
Encode	0	1	EXT	EXT	EXT	– – –	INT	note 2
Decode	1	0	INT	INT	INT	EXT	INT	note 3
Decode	1	1	EXT	EXT	EXT	EXT	INT	

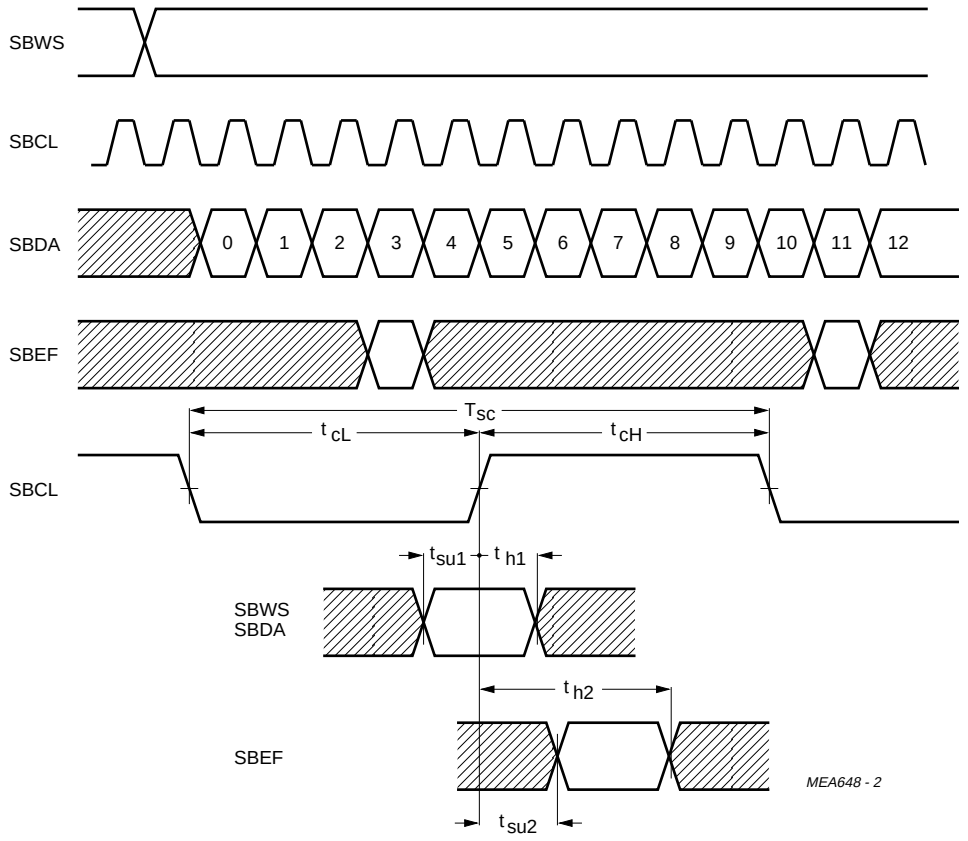
Notes

1. During encoding the SBEF signal is ’don’t care’.
2. Incoming data is not decoded. The SAA2002 operates in the encoding mode and the data does not enter the interface.
3. Operation is undefined. The SAA2002 is in decoding mode whilst the SBWS, SBCL and SBDA output drivers are enabled.



T_s	SBMCLK cycle time	120 to 205 ns (163 ns nominal)
t_{mH}	SBMCLK HIGH time	≥ 35 ns
t_{mL}	SBMCLK LOW time	≥ 75 ns
T_{sc}	SBCL cycle time (384 kbits/s)	$8T_s$ ns nominal
t_{cH}	SBCL HIGH time (384 kbits/s)	≥ $4T_s$ – 20 ns
t_{cL}	SBCL LOW time (384 kbits/s)	≥ $4T_s$ – 20 ns
t_{d1}	SBWS, SBDA hold to SBCL LOW	≤ 20 ns
t_{d2}	SBCL LOW to SBWS, SBDA valid	≤ 20 ns

Fig.15 Sub-band I^2S interface timing (master mode - SBCL, SBWS and SBDA are output).



T_s	SBMCLK cycle time	
T_{sc}	SBCL cycle time	$8T_s$ ns nominal
t_{cH}	SBCL HIGH time	$\geq T_s + 30$ ns
t_{cL}	SBCL LOW time	$\geq T_s + 30$ ns
t_{su1}	SBWS, SBDA input set-up time before SBCL HIGH	$\geq T_s + 30$ ns
t_{h1}	SBWS, SBDA input hold time after SBCL HIGH	≥ 30 ns
t_{su2}	SBCL HIGH to SBEF valid	$\leq T_s - 30$ ns
t_{h2}	SBEF hold time after SBCL HIGH	$\geq 2T_s - 30$ ns

Fig.16 Sub-band I²S interface timing (slave mode - SBCL, SBWS and SBDA are input).

t_{d1}	SBDIR HIGH to SBCL, SBWS SBDA high impedance	≤ 50 ns
t_{d2}	SBCL SBWS, SBDA low impedance after SBDIR LOW	≥ 240 ns

Fig.17 Sub-band I^2S mode switch timing.

Microcontroller interface

The SAA2002 has an interface connection to the serial interface of a microcontroller.

Table 6 Signals used.

SIGNAL	DIRECTION	DESCRIPTION
LTCLK	input	bit clock
LTDATA	bi-directional	serial data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENSFC	input	enable

The SAA2002 microcontroller interface is enabled only if LTENSFC (pin 34) is logic 1. Information to or from the SAA2002 is conveyed in serial 8 or 16-bit units, whilst the type of information is controlled by LTCNT0 (pin 35) and LTCNT1 (pin 36).

A transfer commences when the microcontroller sets the control lines to the correct combination for the required action. LTENSFC is set to logic 1. The SAA2002 determines its required action and prepares to transfer data. When the microcontroller supplies the LTCLK, data is transferred to or from the SAA2002 in units of 8-bits. 16-bit transfers are conveyed as two 8-bit units during which LTENSFC remains HIGH.

During the transfer of 8-bit units, the least significant bit is first to be transferred. When 16-bit units are transferred the most significant byte is sent first

EXTENDED SETTINGS (LTCNT1 = LOGIC 0, LTCNT0 = LOGIC 0)

Four information bits together with four address bits are transferred in this mode. The order in which the bits appear on the interface is:

D0 .. D1 .. D2 .. D3 .. A0 .. A1 .. A2 .. A3

Table 7 Extended settings.

BIT A3	BIT A2	BIT A1	BIT A0	DESCRIPTION
0	0	0	0	CODEC external settings; see Table 8
0	0	0	1	FILTER settings; note 1
0	0	1	0	not used
..	..	..	..	..
1	1	1	1	not used

Note

1.When D0 = logic 1 (default) I^2S mode is selected. For D0 = logic 0 the alternative mode is selected. The setting of D0 remains dormant until activated by the occurrence of FRESET**.**

Table 8 Extended settings.

BIT	DESIGNATION	DEFAULT	DESCRIPTION
D0	MUTEDAC (1)	1	connected to DAC mute input
D1	ATTDAC (1)	0	connected to DAC attenuation input
D2	DEEMDAC (1)	0	emphasis control for DAC circuit
D3	HOLDCLKOK	0	selects CLKOK hold mode

Note

1.If not used for DAC control, the MUTEDAC, ATTDAC and DEEMDAC can be used as general purpose output expanders.

Bits D0 to D3 are copied directly to the corresponding output pins/mode flip-flop.

For HOLDCLKOK = logic 1. When CLKOK drops it will remain low until set by an encode/decode mode, sample frequency, external 256FS or bit rate index change.

ALLOCATION/SCALE FACTOR INFORMATION
(LTCNT1 = LOGIC 0, LTCNT0 = LOGIC 1)

For recording, the allocation and scale factor arrays can be filled using this mode. To completely fill the allocation array 16 complete transfers of 16-bits are required. After the first transfer of allocation information a check must be made to determine when the SAA2002 is ready to receive the remaining information. This will ensure synchronization with the internal program of the SAA2002. Transfer of the allocation information is completed by sending the internal settings.

This is then followed by the scale factor information.

In the event that only internal settings information is sent, then a default allocation of logic 0 will be assigned to all sub-bands. If, in addition no internal settings are sent, then the previous settings remain valid.

The allocation information is transferred in 4-bit units. Each of these units contains the number of bits allocated to the sub-band, MINUS 1, except in the case of a logic 0 value, which indicates that no bits are allocated to that sub-band.

Scale factor information is transferred in units of 8-bits, containing the 6-bit scale factor which is extended to 8- bits by adding two logic 0s at the most significant end.

In the case of stereo encoding the channels are indicated by L (left) and R (right). This changes to I and II in the case of 2 channel mono encoding.

Table 9 Allocation information format.

BITS				CHANNEL	SUB-BAND
MSB			LSB		
B15	B14	B13	B12	L or I	0, 2, 4, ... 30 (even)
B11	B10	B9	B8	R or II	0, 2, 4, ... 30 (even)
B7	B6	B5	B4	L or I	1, 3, 5, ... 31 (odd)
B3	B2	B1	B0	R or II	1, 3, 5, ... 31 (odd)

Table 10 Scale factor information format.

BITS			CHANNEL	SUB-BAND
MSB		LSB		
B15	to	B8	L or I	0 to 31
B7	to	B0	R or II	0 to 31

INTERNAL SETTINGS (LTCNT1 = LOGIC 1, LTCNT0 = LOGIC 0)

The operation of the codec is controlled by the bits transferred in this mode.

Table 11 Internal settings (LTCNT1 = LOGIC 1, LTCNT0 = LOGIC 0).

BITS			NAME	FUNCTION	VALID IN
MSB		LSB			
S15	to	S12	bit rate index	bit rate indication	encode
S11	to	S10	sample frequency	44.1, 48 or 32 kHz indication	encode
S9	–	–	decode	1 = decode, 0 = encode	encode/decode
S8	–	–	EXT 256FS	1 = external; 0 = internal 256FS	encode/decode
S7	–	–	2-channel mono	1 = 2-channel mono; 0 = stereo	encode
S6	–	–	MUTESFC	1 = mute; 0 = no mute	encode/decode
S5	–	–		not used	–
S4	–	–	CH1	1 = CH1; 0 = CH2	decode
S3	to	S2	Tr0 to Tr1	transparent bits	encode
S1	to	S0	EMPHASIS	emphasis indication	encode

Table 12 Internal settings (LTCNT1 = LOGIC 1, LTCNT0 = LOGIC 0).

BITS				BIT RATE	REMARK
MSB			LSB		
1	1	0	0	384 kbits/s	default value

The bit rate index indicates the bit rate of the encoded signal and is only effective in the encode mode.

The decode bit determines the operation mode of the SAA2002. The default value is 1 (decoding mode).

EXT 256FS in the encoding mode determines whether or not the SAA2002 is master or slave of the Filtered-I²S interface (default is 0, master mode).

2-channel mono is used in the encoding mode to determine whether the sub-band signal is generated as a stereo or 2-channel mono signal. Default value is 0.

MUTESFC is used in both the encoding and decoding modes to mute the information to or from the Filtered-I²S interface (the default value is 0).

CH1 is utilized in the decoding mode to select one of the 2-channel mono signals to be decoded (default is 1 channel 1). A value of 0 results in channel 2 being decoded.

The transparent bits are copied in the sub-band signal, default is 00.

The information from S15 to S10, S7 and S3 to S0 will be copied into the sub-band signal.

Table 13 Sample frequency indication.

BITS		SAMPLE FREQUENCY	REMARK
MSB	LSB		
0	0	44.1 kHz	default value
0	1	48 kHz	–
1	0	32 kHz	–
1	1	not used	–

Table 14 EMPHASIS indication.

BITS		EMPHASIS	REMARK
MSB	LSB		
0	0	no emphasis	default value
0	1	50/15 μs	–
1	0	reserved	–
1	1	CCITT J.17	–

Before sending internal settings the microcontroller should check whether or not the SAA2002 is ready-to-receive. However, this does not apply for the transfer of internal settings to end a transfer of allocation information.

STATUS (LTCNT1 = LOGIC1, LTCNT0 = LOGIC 1)

Table 15 Status information 16-bits units.

BITS			NAME	FUNCTION	VALID IN
MSB		LSB			
T15	to	T12	bit rate index	bit rate indication	encode/decode
T11	to	T10	sample frequency	44.1, 48 or 32 kHz indication	encode/decode
T9	–	–	ready-to-receive	1 = ready, 0 = not ready	encode/decode
T8	–	–	not used		
T7	to	T6	MODE	sub-band signal mode indication	encode/decode
T5	–	–	SYNC	synchronization indication	decode
T4	–	–	CLKOK	1 = OK; 0 = not OK	encode/decode
T3	to	T2	Tr0 to Tr1	transparent bits	encode/decode
T1	to	T0	EMPHASIS	emphasis indication	encode/decode

The bit rate index indicates the bit rate of the sub-band signal in units of 32 kbits/s. Bit rate index 0000 indicates the 'free format' condition. Bit rate 1111 is illegal and should not be found.

The coding of the sample frequency indication is equal to the one in the internal settings.

Table 16 MODE identification.

BITS		MODE	OUTPUT
MSB	LSB		
0	0	stereo	L and R
0	1	joint stereo	L and R
1	0	2-channel mono	I or II; as selected
1	1	1-channel mono	mono; no selection

Ready-to-receive indicates whether the SAA2002 is ready to receive allocation, scale factor or internal setting transfers. This should be checked in order to synchronize the transfer of such information.

In 2-channel mono decode mode the selected samples are transferred to both output channels. The same occurs with all samples in 1-channel mono decode mode. In both of these cases the L and R filter output channels are identical.

In decode mode the SYNC bit is logic 0 when the SAA2002 is unable to decode the sub-band frames. This will occur in the following situations:

- With the loss of synchronization.
- When the incorrect allocation information is received for two or more subsequent frames (SBEF was HIGH).
- When the URDA input pin (6) is HIGH.

In these situations the SAA2002 data output will be muted. The SYNC bit will return to logic 1 as soon as the decoder is re-synchronized to the incoming sub-band data.

CLKOK indicates whether the 256FS clock corresponds to specified sample frequency. The CLKOK bit is set to logic 1 after a change in sample frequency, operation mode or EXT256FS setting. It drops to logic 0 as soon as the 256FS clock deviates from the nominal frequency by more than approximately 0.2%. Return to logic 1 will only occur automatically when the extended setting CLKOK-hold-mode is logic 0.

The transparent bits are copied from the PASC signal.

The EMPHASIS indication is as defined in the internal settings. It can be used to apply the correct de-emphasis.

Remark: The two bytes of the status are 'sampled' at different moments so the information may not result from the same sub-band frame.

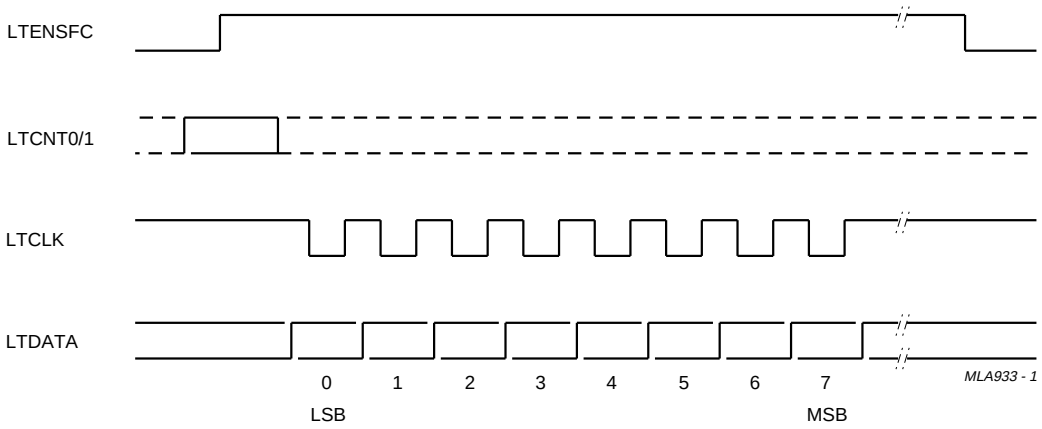


Fig.18 Transfer of data on the SAA2002 microcontroller interface.

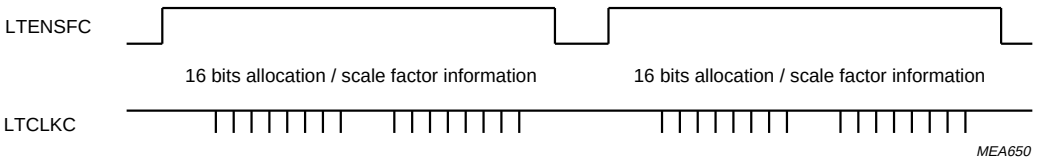


Fig.19 The LTENSFC line must return to logic 0 between information transfers.

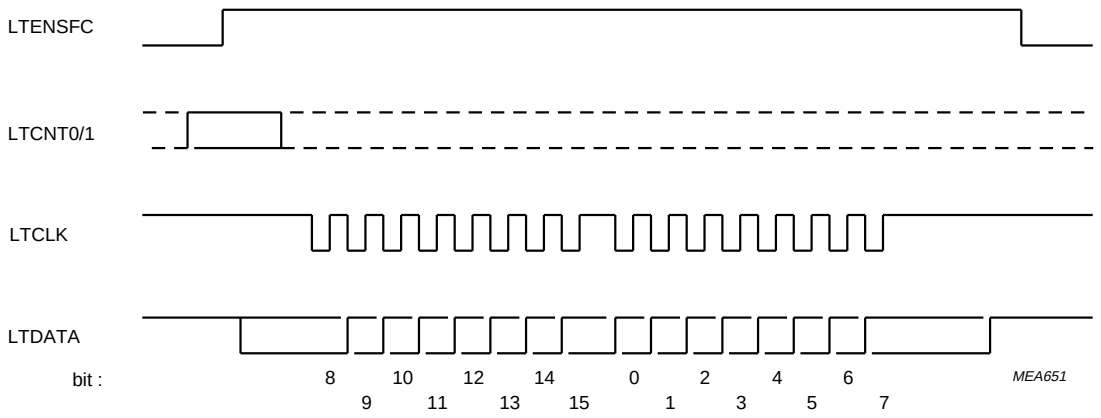
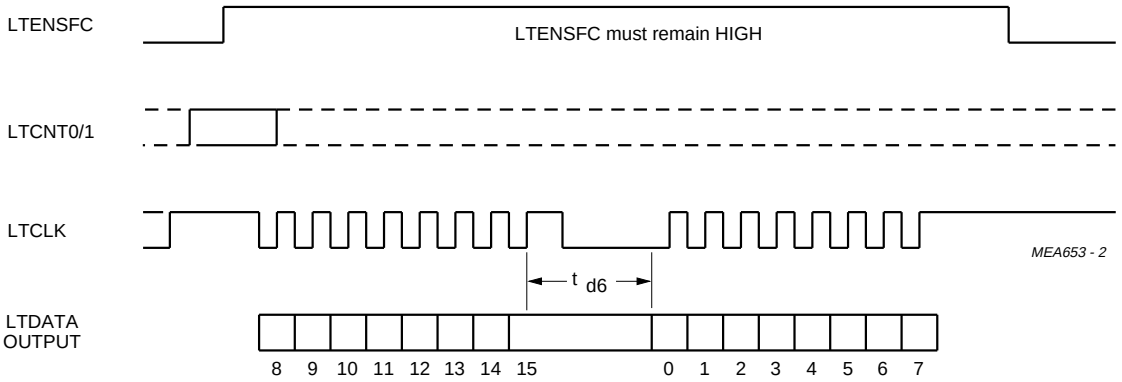
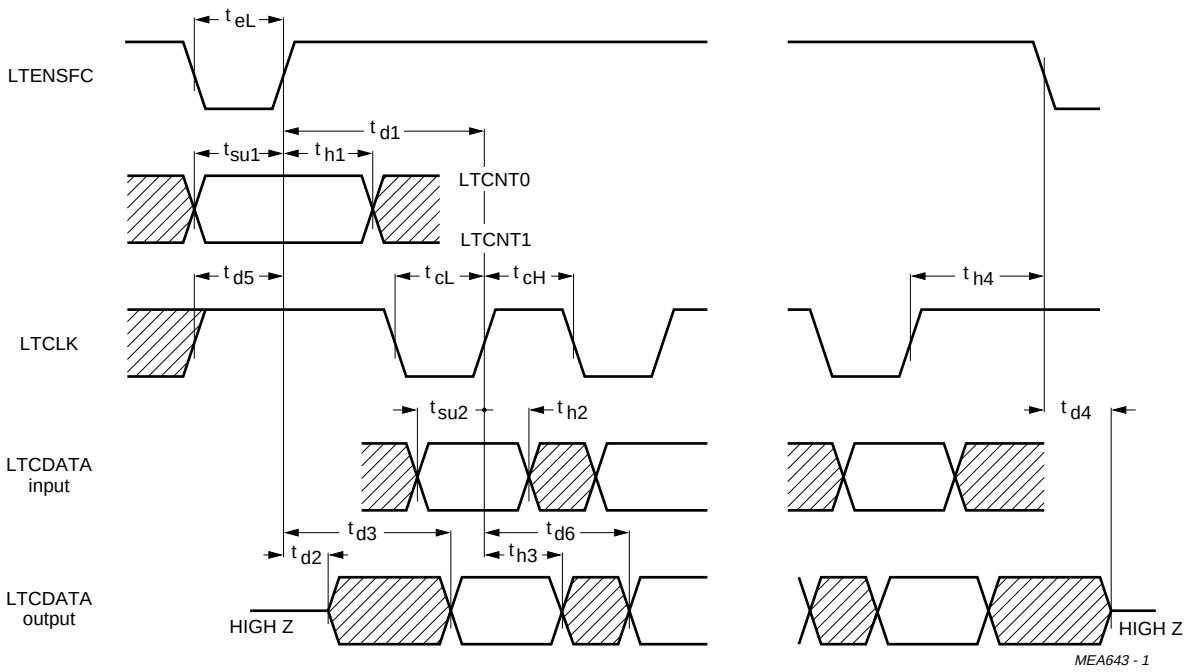


Fig.20 Order of settings and status bits on the SAA2002 microcontroller interface.



t_{d6} delay time LTCLK HIGH to LTDATA valid output for bit 0 in 16-bit transfers.

Fig.21 16-bit transfers.



t_{eL}	LTENSFC LOW time	≥ 190 ns
t_{cH}	LTCLK HIGH time	≥ 190 ns
t_{cL}	LTCLK LOW time	≥ 190 ns
t_{d1}	LTENSFC HIGH to LTCLK HIGH	≥ 190 ns
t_{d2}	LTENSFC HIGH to LTDATA output low impedance	≥ 0 ns
t_{d3}	LTENSFC HIGH to LTDATA output valid	≤ 380 ns
t_{d4}	LTENSFC LOW to LTDATA high impedance	≤ 50 ns
t_{h4}	LTENSFC hold time after LTCLK HIGH	≥ 355 ns
t_{d5}	LTCLK HIGH to LTENSFC HIGH	≥ 190 ns
t_{d6}	LTCLK HIGH to LTDATA output valid; for bit 0 (see Fig.21)	≤ 355 ns
	for bit 8	≤ 520 ns
t_{su1}	LTCNT0/1 set-up time before LTENSFC HIGH	≥ 190 ns
t_{h1}	LTCNT0/1 hold time after LTENSFC HIGH	≥ 190 ns
t_{su2}	LTDATA set-up time before LTCLK HIGH	≥ 190 ns
t_{h2}	LTDATA input hold time after LTCLK HIGH	≥ 30 ns
t_{h3}	LTDATA output hold time after LTCLK HIGH	≥ 145 ns
t_{h4}	LTENSFC hold time after LTCLK HIGH	≥ 355 ns

Fig.22 Microcontroller interface timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_{SS}	supply current in V_{SS}		–	160	mA
I_{DD}	supply current in V_{DD}		–	160	mA
I_I	input current		–10	+10	mA
I_O	output current		–20	+20	mA
P_{tot}	total power dissipation		–	880	mW
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es1}	electrostatic handling	note 2	–1500	+1500	V
V_{es2}	electrostatic handling	note 3	–70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	note 1	3.8	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; note 2	–	82	110	mA
		V_{DD} = 3.8 V; note 2	–	58	80	mA
Inputs URDA, SBDIR, SBEF, LTCLK, LTCNT0, LTCNT1, X22IN and X24IN						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	V_I = 0 V; T_{amb} = 25 °C	–	–	–10	µA
		V_I = 5.5 V; T_{amb} = 25 °C	–	–	10	µA
Inputs PWRDWN and LTENSFC						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	–	V
I_I	input current	V_I = V_{DD}; T_{amb} = 25 °C	40	–	250	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs RESET						
V_{tLH}	threshold voltage LOW-to-HIGH		–	–	$0.8V_{DD}$	V
V_{tHL}	threshold voltage HIGH-to-LOW		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis	$V_{tLH} - V_{tHL}$	–	1.5	–	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	40	–	250	μA
Outputs MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR, FRESET, FSYNC and CLK22						
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
Output CLK24						
V_{OL}	LOW level output voltage	I_O = –8 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 8 mA	V_{DD} – 0.5	–	–	V
Inputs/outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA and LTDATA						
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
Outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA and LTDATA in 3-state						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	40	–	250	μA
Input/output SBMCLK						
V_{OL}	LOW level output voltage	I_O = –8 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 8 mA	V_{DD} – 0.5	–	–	V
Output SBMCLK in 3-state						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	40	–	250	μA
Input/output FS256						
V_{OL}	LOW level output voltage	I_O = –12 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 12 mA	V_{DD} – 0.5	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output FS256 in 3-state						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	40	–	250	μA

Notes

1. For applications requiring minimum power dissipation the device may be operated from a nominal +4 V supply.
2. For load impedances representative of the application.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
C_I	input capacitance		–	–	10	pF
X24IN and X22IN						
f_{xtal}	crystal frequency at X22OUT, CLK22	note 1	21	22.5792	24	MHz
f_{xtal}	crystal frequency at X24OUT, CLK22	note 1	23	24.576	26	MHz
g_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
A_v	small signal gain	$A_v = g_m.R_o$	3.5	–	–	V/V
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Outputs						
C_O	output capacitance		–	–	10	pF
Inputs URDA, RESET, LTDATA, LTCLK, LTENSFC, LTNT0 and LTNT1						
t_{su}	set-up time to X24IN		15	–	–	ns
t_h	hold time to X24IN		60	–	–	ns
Outputs LTDATA, MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR and FRESET						
t_{PD}	propagation delay time from X24IN		–	–	80	ns
Inputs FDAF, FDAC, SDA, SCL and SWS						
t_{su}	set-up time to FS256		15	–	–	ns
t_h	hold time to FS256		25	–	–	ns

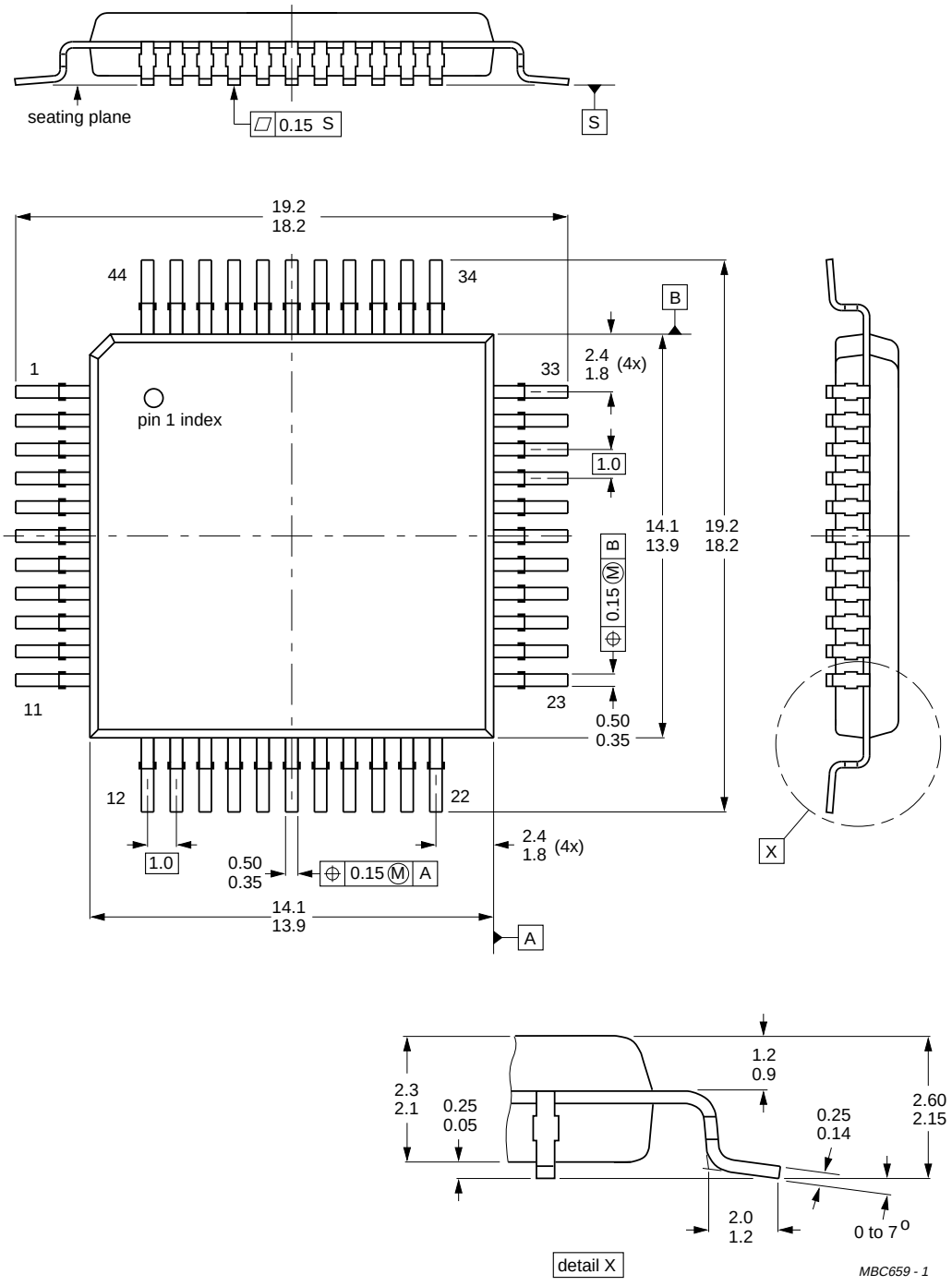
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs FDAF, FDAC, SDA, SCL, SWS and FSYNC						
t_{PD}	propagation delay time from FS256		–	–	50	ns
Inputs SBDA, SBCL, SBWS, URDA, SBDIR and SBEF						
t_{su}	set-up time to SBMCLK		15	–	–	ns
t_h	hold time to SBMCLK		25	–	–	ns
Outputs SBDA, SBCL and SBWS						
t_{PD}	propagation delay time from SBMCLK		–	–	50	ns
FS256						
T	FS256 cycle time	f_s = 48 kHz	–	81.4	–	ns
		f_s = 44.1 kHz	–	88.6	–	ns
		f_s = 32 kHz	–	122.1	–	ns
T_c	SCL cycle time		–	4T	–	ns
FS256 master mode (FS256, SCL and SWS are output)						
t_{fH}	FS256 HIGH time	f_s = 48 kHz	35	–	–	ns
		f_s = 44.1 kHz	38	–	–	ns
		f_s = 32 kHz	75	–	–	ns
t_{fL}	FS256 LOW time	f_s = 48 kHz	35	–	–	ns
		f_s = 44.1 kHz	38	–	–	ns
		f_s = 32 kHz	75	–	–	ns
t_{sH}	SCL HIGH time		2T – 20	–	–	ns
t_{sL}	SCL LOW time		2T – 20	–	–	ns
t_{su}	SDA, FDAF, FDAC input set-up time before FS256 HIGH		20	–	–	ns
t_{h1}	SDA, FDAF, FDAC input hold time after FS256 HIGH		30	–	–	ns
t_{h2}	SDA, FDAF, FDAC output hold time after FS256 HIGH		0	–	–	ns
$t_{d1,2}$	FS256 HIGH to SCL, SWS, SDA, FDAF, FDAC output valid		–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FS256 slave mode (FS256, SCL and SWS are input)						
t_{fH}	FS256 HIGH time		35	–	–	ns
t_{fL}	FS256 LOW time		35	–	–	ns
t_{sH}	SCL HIGH time		T + 35	–	–	ns
t_{sL}	SCL LOW time		T + 35	–	–	ns
t_{h1}	SDA, FDAF, FDAC output hold time after SCL HIGH		2T – 15	–	–	ns
t_{d}	SCL HIGH to SDA, FDAF, FDAC output valid		–	–	3T + 60	ns
t_{su}	SDA, FDAF, FDAC input valid after SCL HIGH		20	–	–	ns
t_{h2}	SDA, FDAF, FDAC input hold time after SCL HIGH		T + 20	–	–	ns
SBMCLK						
T_{s}	SBMCLK cycle time		120	163	205	ns
t_{mH}	SBMCLK HIGH time		35	–	–	ns
t_{mL}	SBMCLK LOW time		75	–	–	ns
SBMCLK master mode (SBCL, SBWS and SBDA are output)						
T_{sc}	SBCL cycle time	384 kbits/s	–	$8T_s$	–	ns
t_{cH}	SBCL HIGH time	384 kbits/s	$4T_s$ – 20	–	–	ns
t_{cL}	SBCL LOW time	384 kbits/s	$4T_s$ – 20	–	–	ns
t_{d1}	SBWS, SBDA hold	to SBCL LOW	20	–	–	ns
t_{d2}	SBWS, SBDA valid	after SBCL LOW	–	–	20	ns
SBMCLK slave mode (SBCL, SBWS and SBDA are input)						
T_{sc}	SBCL cycle time		–	$8T_s$	–	ns
t_{cH}	SBCL HIGH time		T_s + 30	–	–	ns
t_{cL}	SBCL LOW time		T_s + 30	–	–	ns
t_{su1}	SBWS, SBDA set-up time	before SBCL HIGH	T_s + 30	–	–	ns
t_{h1}	SBWS, SBDA hold time	after SBCL HIGH	30	–	–	ns
t_{su2}	set-up time before SBEF valid	after SBCL HIGH	–	–	T_s – 30	ns
t_{h2}	SBEF hold time	after SBCL HIGH	$2T_s$ – 30	–	–	ns

Notes

1. Percentage deviation from nominal frequency must be the same for X24, X22 and FS256 inputs within 0.2%.
2. For applications requiring minimum power dissipation the device may be operated from a nominal +4 V supply.

PACKAGE OUTLINE



Dimensions in mm.

Fig.23 44-lead quad flat-pack; plastic (SOT205AG).

SOLDERING

Quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two waves (dual-wave), in which, in a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress rating only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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