1 PRODUCT OVERVIEW

SAM87RI PRODUCT FAMILY

Samsung's SAM87RI family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A dual address/data bus architecture and a large number of bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM87RI microcontrollers have an external interface that provides access to external memory and other peripheral devices.

KS86C0004/P0004/C0104/P0104 MICROCONTROLLER

The KS86C0004/P0004/C0104/P0104 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87RI CPU core.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The KS86C0004/P0004/C0104/P0104 has 4 K bytes of program memory on-chip.

Using the SAM87RI design approach, the following peripherals were integrated with the SAM87RI core:

— Five configurable I/O ports (32 pins)

— 12 bit-programmable pins for external interrupts

— 8-bit timer/counter with three operating modes

The KS86C0004/P0004/C0104/P0104 is a versatile microcontroller that can be used in a wide range of general purpose applications. It is especially suitable for use as a keyboard controller and is available in a 40-pin DIP and a 44-pin QFP package.

OTP

The KS86C0004/C0104 microcontroller is also available in OTP (One Time Programmable) version, KS86P0004/P0104. KS86P0004/P0104 microcontroller has an on-chip 8-Kbyte one-time-programmable EPROM instead of masked ROM. The KS86P0004/P0104 is comparable to KS86C0004/C0104, both in function and in pin configuration.

FEATURES

CPU

- SAM87RI CPU core

Memory

- 4-Kbyte internal program memory (ROM)
- 208-byte internal register file
- 8-Kbyte external program memory
- 8-Kbyte external data memory

Instruction Set

- 41 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 1.5 µs at 4 MHz f_{OSC}

Interrupts

- 14 interrupt sources with one vector, Each source has its pending bit
- One level, one vector interrupt structure

Oscillation Circuit Options

- 4 MHz RC oscillator with on chip capacitor for **KS86C0004/P0004** (± 10% RC accuracy at V_{DD} ± 5% and Ta = 0°C – 70°C, using 1% external precision resistor)
- RC oscillator for **KS86C0004/P0004**
- Crystal/ceramic oscillator for **KS86C0104/P0104**

General I/O

- Five ports (32 pins total)
- Three bit-programmable ports (20 pins total)
- Two bit-programmable ports with external interrupts (12 pins total)

Timer/Counter

- One 8-bit basic timer for watchdog function and programmable oscillation stabilization interval generation function
- One 8-bit timer/counter with PWM mode

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 4.5 V to 5.5 V for KS86C0004/P0004
- 2.7 V to 5.5 V for KS86C0104/P0104

Package Types

- 40-pin DIP

BLOCK DIAGRAM

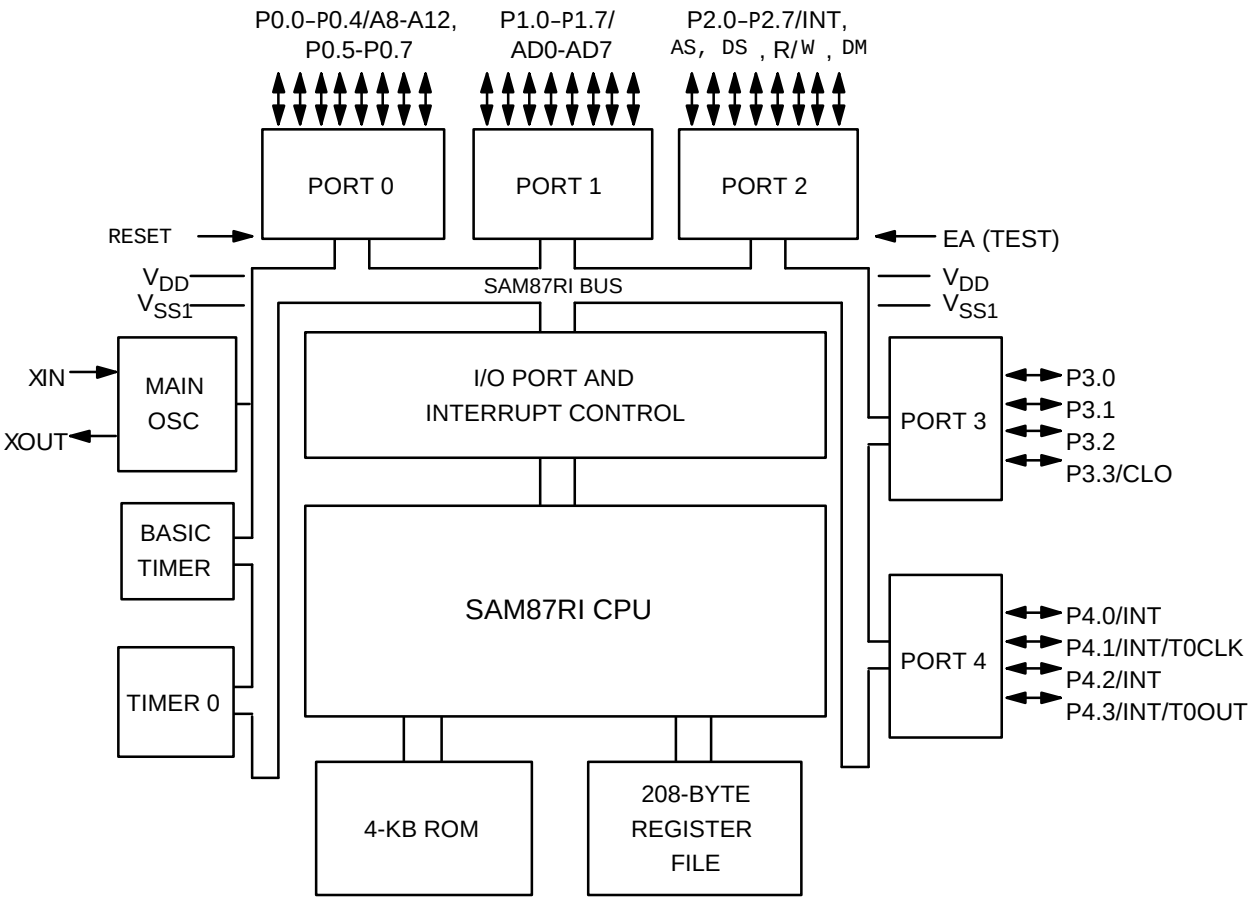


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

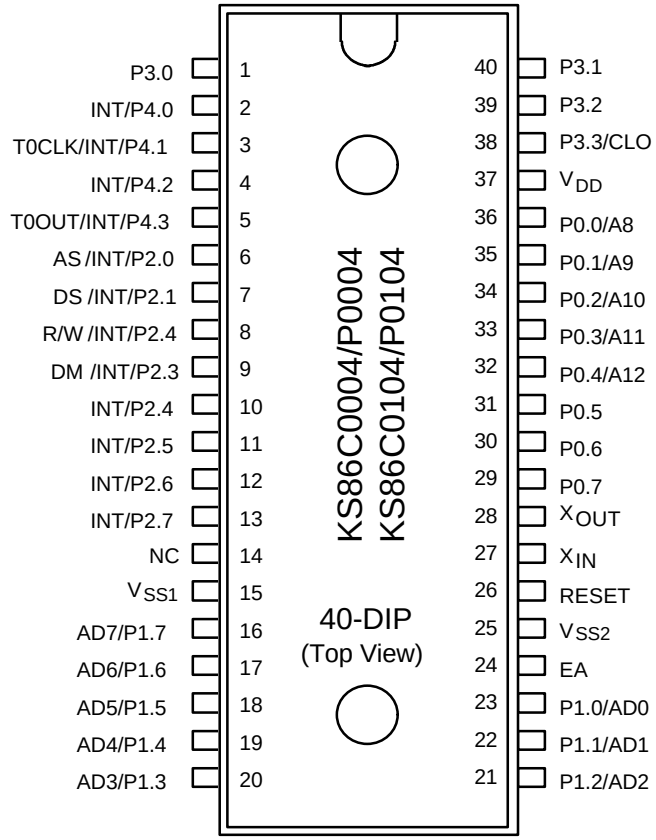


Figure 1-2. Pin Assignment Diagram (40-Pin DIP Package)

PIN DESCRIPTIONS

Table 1-1. KS86C0004/P0004/C0104/P0104 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Number	Pin Numbers	Share Pins
P0.0–P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port0 can also be configured as external interface address lines A8–A12.	C	36–29	A8–A12
P1.0–P1.7	I/O	Bit-programmable I/O port for Schmitt trigger input, push-pull, or open-drain output. Port1 can alternatively be used as external interface address/data lines AD0–AD7.	C	23–16	AD0–AD7
P2.0–P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Port2 can be individually configured as external interrupt inputs. Especially, P2.0–2.3 can be configured for external bus control signal.	D	6–13	INT, AS, DS, R/W, DM
P3.0–P3.3	I/O	Same general characteristics as Port1. Port3 are designed for to drive LED directly. P3.3 can be used to system clock output (CLO) port.	C	1, 40–38	P3.3/CLO
P4.0–P4.3	I/O	Bit-programmable I/O port. Input mode or n-channel open-drain output mode is software assignable. Port4 can be individually configured as external interrupt inputs. Pull-up resistors are also software assignable. Especially, P4.1 can be used T0CLK input and P4.3 also T0OUT for Timer 0.	D	2–5	INT, T0CLK, T0OUT
X_{IN}, X_{OUT}	–	System clock input and output pin (for RC oscillator, crystal/ceramic oscillator, or external clock source)	–	27, 28	–
INT	I	External interrupt for bit-programmable port2 and port4 pins when set to input mode.	–	2-13	PORT2/ PORT4
RESET	I	RESET signal input pin. Schmitt trigger input with internal pull-up resistor.	A	26	–
EA	I	External Memory Access (EA) pin with 2 modes: 0V = Normal Operation Mode 5V = ROMLESS Operation Mode (Must be connected to V_{SS} during normal operation mode)	B	24	–
V_{DD}	–	Power input pin	–	37	–
V_{SS1}, V_{SS2}	–	Vss1 is a ground power for CPU core. Vss2 is a ground power for I/O and OSC block	–	15, 25	–
NC	–	No connection (This pin would be better connecting to V_{SS})	–	14	–

PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the KS86C0004/P0004/C0104/P0104

Circuit Number	Circuit Type	KS86C0004/P0004/C0104/P0104 Assignments
A	I	RESET signal input
B	I	EA input
C	I/O	Ports 0, 1, and 3
D	I/O	Ports 2 and 4

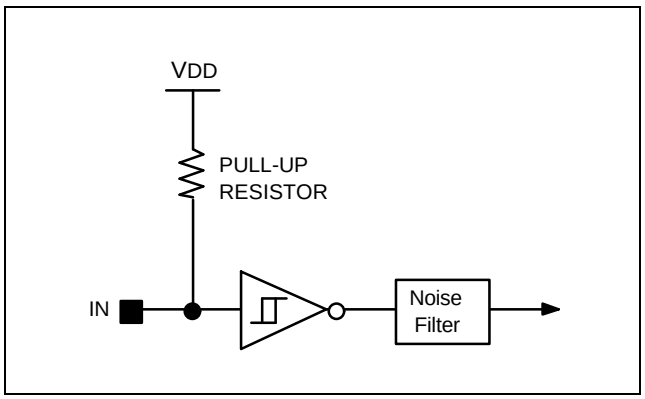


Figure 1-3. Pin Circuit Type A (RESET)

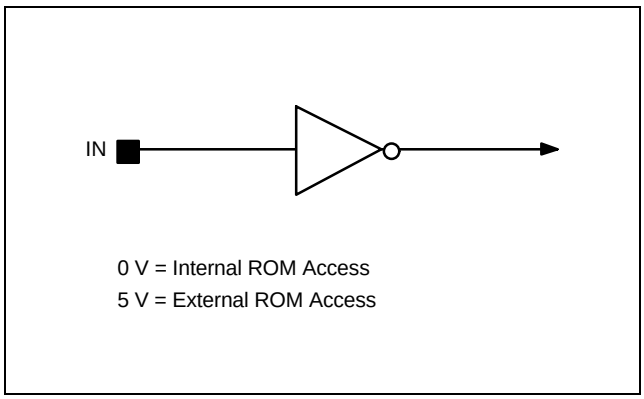
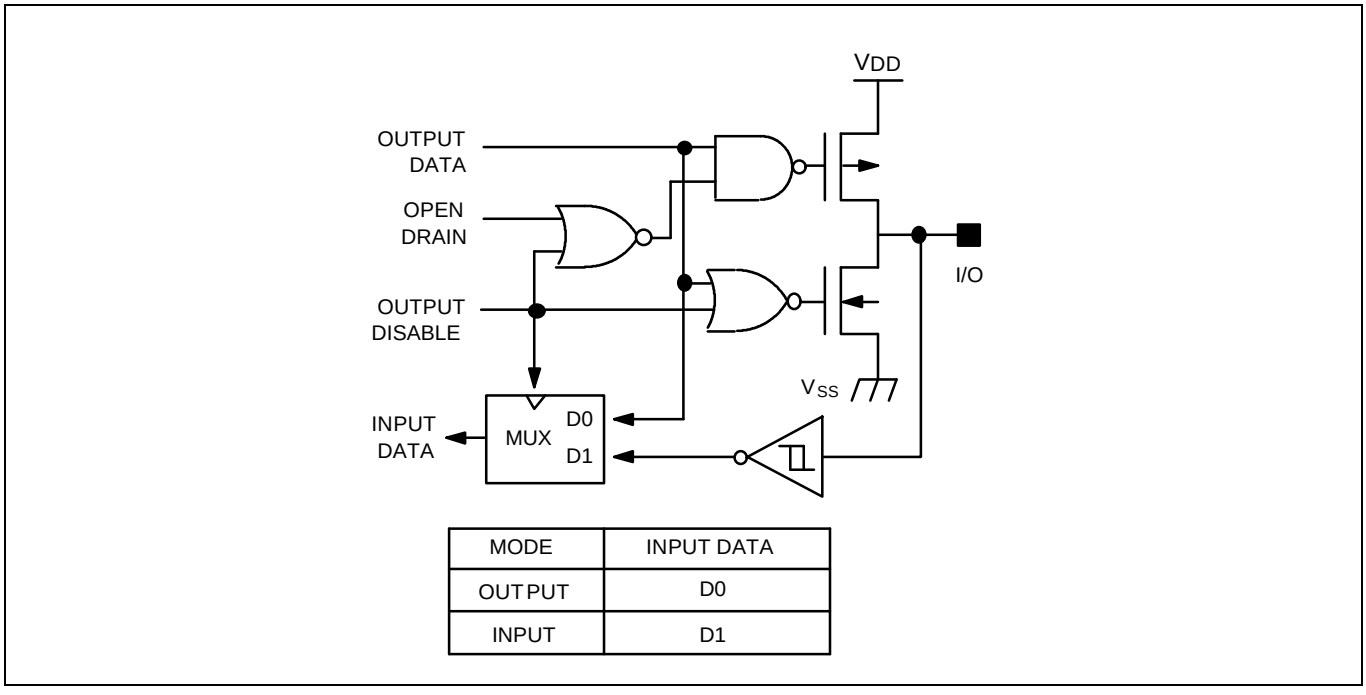


Figure 1-4. Pin Circuit Type B (EA)



MODE	INPUT DATA
OUTPUT	D0
INPUT	D1

Figure 1-5. Pin Circuit Type C (Ports 0, 1, and 3)