

DUAL SPDT CMOS/D-MOS ANALOG SWITCHES WITH DATA LATCHES

ORDERING INFORMATION

	16-Pin Plastic DIP	SO-16 Surface Mount
Commercial Temp. Range	CDG2269CJ	CDG2269CY
Package Dimensions	See Package 10	See Package 21

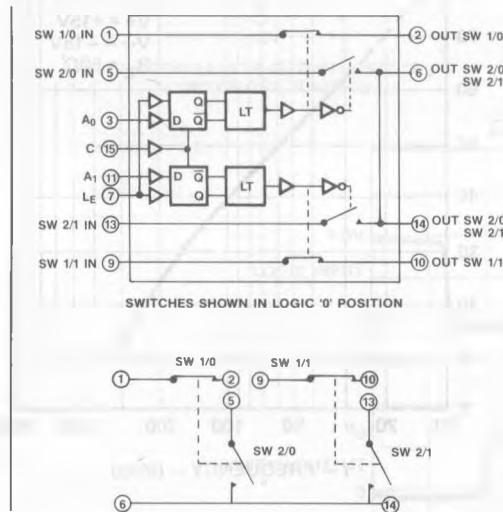
FEATURES

- High OFF Isolation
- Low Channel-to-Channel Crosstalk
- Wide Bandwidth
- Analog Signal Range +10V to -10V
- Low ON Resistance, 20Ω typ.

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Switches feature high-speed, low-power 5 volt CMOS input logic and level translation circuitry are fabricated together on a single silicon chip. This part is designed for applications where high "off" isolation at high frequencies is needed.

LOGIC DIAGRAM



APPLICATIONS

- RF & Video Switches
- High Speed Precision Data Acquisition
- L-PAD Digital Controlled Attenuators

NOTE

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{CC} or GND).

FUNCTION TABLE

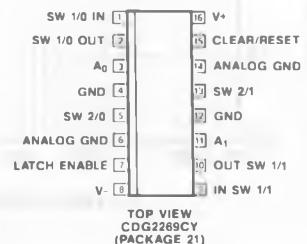
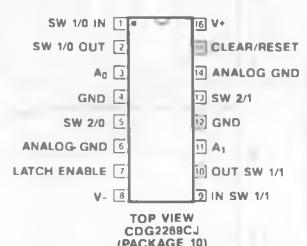
INPUT			SWITCH	
A	L _E	C	SW ₁	SW ₂
L	H	L	ON	OFF
H	H	L	OFF	ON
X	X	H	OFF	ON
L	L	L	*(1)	*(2)

X = undefined

*(1) Hold input state one setup before L_E High to Low transition. If Input state Low then Switch ON. If Input state High then Switch OFF.

*(2) SW₁ = SW₂

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

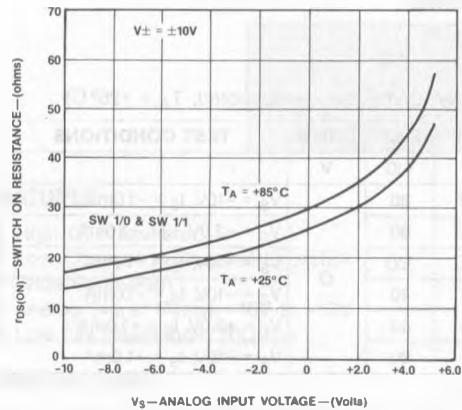
V-	Negative Supply Voltage	-20V
V+	Positive Supply Voltage	+20V
V _{IN}	Control Input Voltage Range	V+ +0.3V, V- -0.3V
I _L	Continuous Current, any Pin except S or D	20mA
I _S	Continuous Current, S or D	30mA
I _S	Peak Pulsed Current, S or D, 80μsec, 1%	
Duty Cycle		100mA
T _J	Junction Temperature Range	-55 to +125°C
T _S	Storage Temperature Range	-55 to +125°C
P _D	Power Dissipation	500mW

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel, unless otherwise noted, T_A = +25°C)

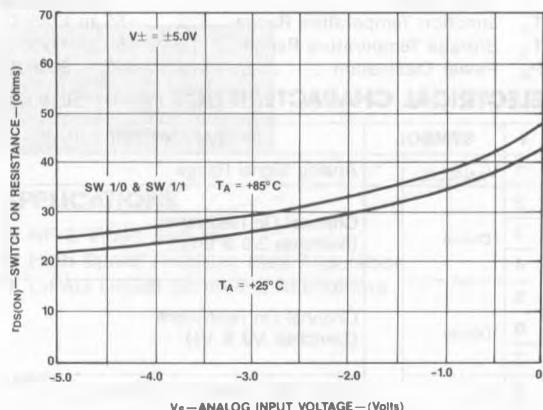
#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V _{ANALOG}	Analog Signal Range	-10		+10	V	STATIC
2		Channel On Resistance (Switches 2/0 & 2/1)		29	80	Ω	V _S = -10V, I _S = -1.0mA
3	r _{DS(on)}			40	80		
4				100	160		
5		Channel On Resistance (Switches 1/0 & 1/1)		13	40	Ω	V _S = +10V, I _S = +1.0mA
6	r _{DS(on)}			20	40		
7				50	80		
8	V _{IH}	Logic High Level Input Voltage	4.5	3.4		V	V _S = +2.0V, I _S = +1.0mA
9	V _{IL}	Logic Low Level Input Voltage			1.0		
10	I _{IN}	Logic Input Leakage Current		0.01	0.1	μA	V _{IN} = +5.0V
11				0.02	0.1		V _{IN} = +15V
12	I _{D(OFF)}	Switch OFF Leakage Currents (Switches 2/0 & 2/1)		0.4	5.0	nA	V _D = +10V, V _S = -10V
13	I _{S(OFF)}			4.0	20		V _S = +10V, V _D = -10V
14	I _{D(OFF)}			0.4	5.0		V _D = +10V, V _S = -10V
15	I _{S(OFF)}			4.0	20		V _S = +10V, V _D = -10V
16	I-	Negative Supply Quiescent Current	-0.05	-0.5		μA	V _{IN} = 0 or V+
17	I+	Positive Supply Quiescent Current	.03	0.5			
18		Propagation Delay	Data to Switch ON	180	250	nSec	
19			Data to Switch OFF	100	200		
20			Latch Enable to Sw. ON	180	250		
21			Latch Enable to Sw. OFF	140	200		
22			Clear to Switch ON	180	250		
23			Clear to Switch OFF	90	150		
24	t _S	Set Up Time	150	120		dB	
25	t _H		150	90			
26	P _W	Pulse Width	50	40			
27	O _{IRR}	OFF Isolation Rejection Ratio (Switches 1/0 & 1/1)	42	45			f = 10MHz R _L = 50Ω
28			12	15			
29		Frequency Roll-Off (Bandwidth)	1.0	3.0			f = 200MHz, R _L = 50Ω
30	I _L	Insertion Loss (Switches 1/0 & 1/1)	2.0				f = 10MHz R _L = 50Ω
31			3.0				f = 200MHz R _L = 50Ω
32	C _d	Drain-Node Capacitance	0.6			pF	V _D = 0 f = 1MHz, V _{IN} = 0
33	C _s	Source-Node Capacitance	6.0				

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

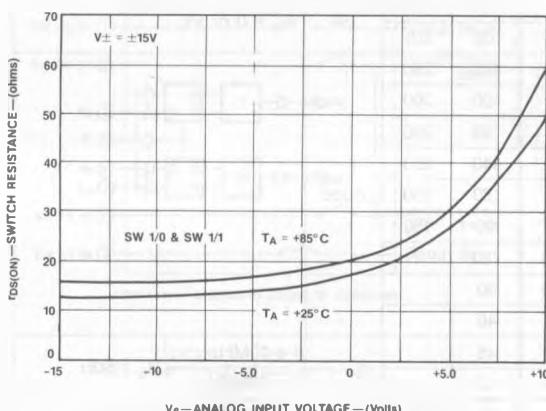
**SWITCH ON RESISTANCE
—vs—
ANALOG INPUT VOLTAGE**



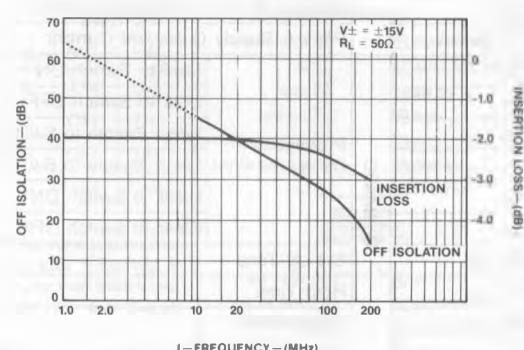
**SWITCH ON RESISTANCE
—vs—
ANALOG INPUT VOLTAGE**



**SWITCH ON RESISTANCE
—vs—
ANALOG INPUT VOLTAGE**



**OFF ISOLATION & INSERTION LOSS
—vs—
FREQUENCY**



TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

